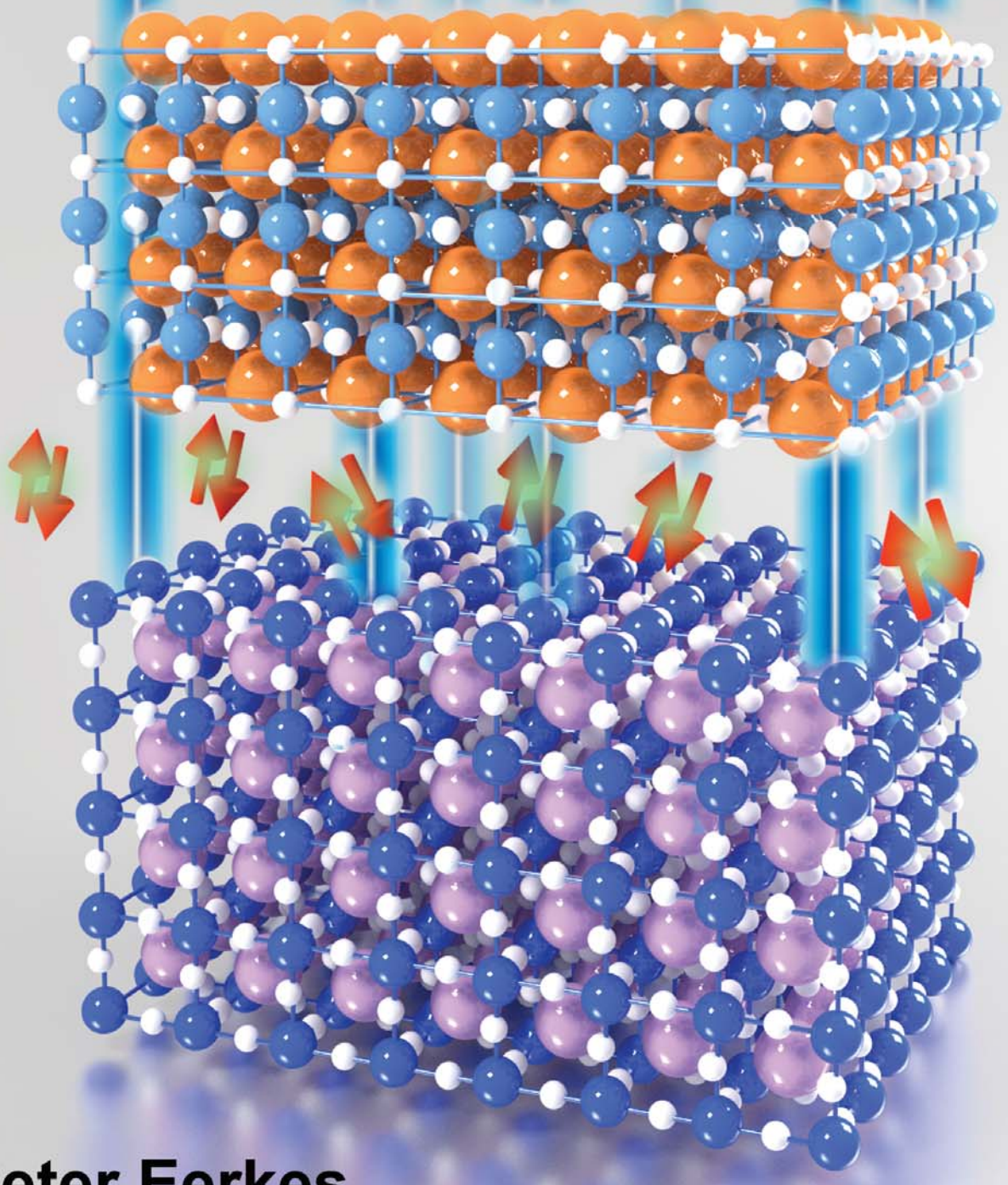
Top-gating of the two-dimensional electron gas at complex oxide interfaces



Peter Eerkes

TOP-GATING OF THE TWO-DIMENSIONAL ELECTRON GAS AT COMPLEX OXIDE INTERFACES

Peter Eerkes

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Cover: artist impression of the influence of an electric field on Cooper pairs at the interface between $LaAlO_3$ and $SrTiO_3$. Design by Xiao Renshaw Wang.

The work described in this thesis was carried out at the Nano Electronics group at the Faculty of Electrical Engineering, Mathematics and Computer Science, and the Interfaces and Correlated Electron Systems group at the Faculty of Science and Technology, and the MESA+ Institute for Nanotechnology, P.O. Box 217, 7500 AE Enschede, the Netherlands.
This research was supported by the Dutch Foundation for Research on Matter (FOM) through the InterPhase program.

Peter Eerkes
Top-gating of the two-dimensional electron gas at complex oxide interfaces
Ph.D. thesis University of Twente, Enschede, the Netherlands.

ISBN 978-90-365-3655-4
DOI: 10.3990/1.9789036536554

Printed by: Gildeprint Drukkerijen

TOP-GATING OF THE TWO-DIMENSIONAL ELECTRON GAS AT COMPLEX OXIDE INTERFACES

PROEFSCHRIFT

ter verkrijging van
de graad van doctor aan de Universiteit Twente,
op gezag van de rector magnificus,
prof. dr. H. Brinksma
volgens besluit van het College voor Promoties
in het openbaar te verdedigen
op donderdag 19 juni 2014 om 14.45 uur

door

Pieter Dirk Eerkes

geboren op 18 November 1985
te Zwolle

Dit proefschrift is goedgekeurd door de promotoren:

Prof. dr. ir. H. Hilgenkamp
Prof. dr. ir. W.G. van der Wiel

Table of Contents

Chapter 1

Introduction and motivation

This chapter gives a short introduction and motivation to the work described in this thesis

1.1 Introduction

Since ancient times it has been known that combining raw materials may lead to a new material with different, and, if well designed, better properties. One of the first alloys made between 4000 and 5000 years ago, was bronze, an alloy of tin and copper. Bronze replaced flint, stone, as the work horse material. Since bronze can be casted, this gave a huge improvement in design and quality of weapons and tools. In 5000 years the knowledge about materials and the technology to make them improved a lot. Nowadays materials can be deposited as thin films in ultra-high vacuum using techniques as e-beam evaporation, pulsed laser deposition (PLD) and molecular beam epitaxy (MBE). Furthermore, techniques such as reflective high energy electron diffraction (RHEED) allow for monitoring and control at the unit cell (u.c.) level. One of the combinations of materials that only can be made using these kinds of techniques is the combination of $SrTiO_3$ (STO) and $LaAlO_3$ (LAO). These materials are insulating in the bulk, however, when these are combined, the interface between these materials becomes conducting and depending on the specific growth conditions superconducting or magnetic. The origin of these properties will not be the main topic of this thesis, although they will be briefly discussed. The goal of the research described in this thesis is to fabricate high quality top-gated electric field effect devices with these novel oxide two-dimensional conducting systems. When we succeed to produce these, we can investigate the influence of top-gating on some of the intriguing properties of these oxide interfaces.

1.2 Motivation

When I started my phd-research in 2010, quite a lot of the interesting properties of the LAO/STO system were already discovered and they could be tuned using an electric field, by applying a back-gate voltage. A clear disadvantage of a back-gate, is the fact that is a global technique, the carrier density in the whole sample is changed when an electric field is applied from the back-side of the sample. Furthermore, the voltages that need to be used are large (hundreds of Volts), due to the thickness of the STO-substrate (typically 0.5-1 mm). STO has a cubic crystal structure at room temperature, however when the crystal is cooled below T = 105 K, it undergoes a structural transition to the tetragonal phase[1]. Recently it has been discovered that the tetragonal domains in the STO-substrate start moving when an electric field is applied across it. [2] [3, 4] This movement of the domains causes a change in the conductivity at the surface of the STO (at the interface between LAO and STO). The interface conductivity may also be altered by oxygen vacancies in the STO, that can move when a large voltage is applied across it. So applying a back-gate voltage, changes more than just the carrier density and properties associated with it.

In order to resolve these problems, I have developed a technique to construct top-gates on LAO/STO. Using top-gating, the electric field is applied across the LAO, so the domains

in STO do not move, because they do not experience an electric field. Smaller voltages can be used, since the electron gas is very close (about 4 nm) to the top-electrode. The key motivation for enabling top-gating was, however, the ability to have local control over the electron gas.

1.3 Thesis outline

After this introduction, chapter 2 will be a small review about the experimental work that has been performed in the last 10 years, since the discovery of the conducting two-dimensional electron gas (2DEG) at the interface between two non-conducting oxide perovskites. The focus will be on the material science and electronic transport measurements, topics that are the closest to the work I did myself. In chapter 3 the growth of the LAO/STO and the road towards top-gating them will be described. Chapter 4 shows electrical measurements on top-gated LAO/STO interfaces that have been conducted at room temperature. Chapter 5 will cover electrical measurements at low temperatures, focussing on the tuning of the superconductivity by applying a small gate voltage. Chapter 6 demonstrates that the spin-orbit coupling of the conductance electrons at the oxide interfaces can be tuned by applying a top-gate voltage.

Chapter 2

Properties and origin of the two-dimensional electron gas between $LaAlO_3$ and $SrTiO_3$

This chapter summarizes the most important experimental work done in one decade of research on conductivity between two insulating complex oxides. It is not intended to be complete, however it gives the reader a good starting point to understand the developments and current state of the field of complex oxides.

2.1 Introduction

Oxide perovskites can be described by the general formula ABO_3. These perovskites consist of, next to oxygen atoms as the name suggests, two different elements. 'A' is an alkaline earth metal (Be, Mg, Ca, Sr, Ba, Ra) or rare earth metal (for example Sc, Y, La, Gd, Dy) element and 'B' is a transition metal (Sc, Ti, V, Mn, Fe, etc.) or a poor metal (Al, Ga, Pb, Sn, Tl, In) element. The perovskite structure consists of alternating layers of AO and BO_2. Most of these materials are transparent and insulating, being either band insulators or Mott insulators.

It was a surprise when Ohtomo and Hwang[5] found conductivity at the interface between two prominent members of the oxide perovskite group: $SrTiO_3$ (STO) and $LaAlO_3$ (LAO), where a two-dimensional electron gas (2DEG) forms at the interface. Both STO and LAO can be regarded as wide-band-gap insulators (bulk values: STO = 3.2 eV, LAO = 5.6 eV). Since the lattice mismatch between these materials is small (STO = 3.789 Å, LAO = 3.905 Å), LAO can be grown epitaxially on STO. When LAO is grown on TiO_2-terminated STO, the interface becomes highly conducting, whereas LAO grown on SrO-terminated STO does not lead to a conducting interface[6].

Conductivity between insulating oxides not only occurs at the LAO/STO interface. Growing for example $LaTiO_3$ [7], $LaGaO_3$ [8], $LaCrO_3$ [9], $DyScO_3$ [10], $GdTiO_3$ [11] or amorphous oxides[12, 13] on $SrTiO_3$ also results in a conducting interface. However, most of the research has been performed on LAO/STO, which can be seen as a model system for all 2DEGs formed at the interface between complex oxides, because the physics and properties of the 2DEGs are similar for all these materials on STO.

In the first part of this chapter, the basic properties of the LAO/STO will be discussed, followed by an analysis: can it be explained where the electronic properties originate from? The results of an experimental study that can shine light on this question are discussed in section 2.4. The experiment using hard x-ray spectroscopy has been performed together with E. Slooten and Prof. M.S. Golden (University of Amsterdam). This is followed by a part that discusses electronic devices in this kind of materials, as an introduction to the experimental work in this thesis.

2.2 Properties of the STO/LAO interface

One of the experiments that really started the interest in research on the interface conductivity after its discovery, was the one performed by Thiel *et al.*[14] They reported that conductivity at the interface abruptly appears when the LAO that is deposited on STO equals or exceeds a critical thickness of 4 unit cells (u.c.). It was also shown that an electric field could tune a, normally insulating, 3 u.c. LAO/STO sample conducting when a positive back-gate voltage was applied.

The carrier (electron) density n_s of the LAO/STO 2DEG is about $2x10^{13}$ cm^{-2} at low temperatures (2K). At room temperature n_s is higher, in the order of $1x10^{14}$ cm^{-2}, upon cooling down there is a so-called carrier freeze out. The amount of carriers can be different when an additional layer is deposited on top of the LAO, such as YBaCuO (YBCO), that lowers the carrier density to about 10% of its original value.[15] A capping of SrCuO/STO gives a similar value[16] as YBCO whereas a capping of $La_{1-x}Sr_xMnO_3$ gives a lower carrier density that scales with the strontium amount[17] *x.*

The usual carrier mobility (μ) is about 200-2,000 cm^2/Vs at low temperatures (2K) at conventional LAO/STO interfaces. Unlike the carrier density, which is very reproducible. The low temperature mobility is mainly determined by defect scattering. This defect density can vary strongly from substrate to substrate, as a result the mobility can vary about an order of magnitude from sample to sample. Similar to n_s, μ can be influenced by changing the LAO surface with a capping layer[15, 16] or surface adsorbents[18].

It is possible to produce samples with a higher mobility, this can been done optimizing the growth of the LAO[19] or by adding additional capping layers on top of the LAO[16]. These procedures result in a better penetration of oxygen into the sample, reducing the number of oxygen vacancies, which can act as scatter centers.[16] When the mobility is high enough (exceeding about 5,000 cm^2/Vs) Shubnikov-de Haas (SdH) oscillations can be observed[19, 20]. These Shubnikov-de Haas oscillations can be observed in the longitudinal resistance as a function of perpendicular magnetic field. The oscillations originate from the fact that electrons under influence of the magnetic field move in a cyclotron motion. Due to the wave nature of the electrons this leads to quantization, which is visible in the resistance. These oscillations are periodic in $1/B$ (B is the applied perpendicular magnetic field) when conventional LAO/STO samples with optimized growth conditions have a high enough mobility. When a capping layer is used, a multiband character of the oscillations is observed; 4 or 5 types of charge carriers with different effective masses and mobility are needed to describe the oscillations[21]. It should be mentioned that the original paper from Ohtomo and Hwang also mentioned the observation of SdH oscillations[5]. However, as we now understand, the growth pressure they used for the LAO deposition was too low, leading to oxygen vacancies in the STO, which made the bulk STO a (three dimensional) conductor. The observed SdH oscillations originated from this bulk conductivity and were not an interface property.

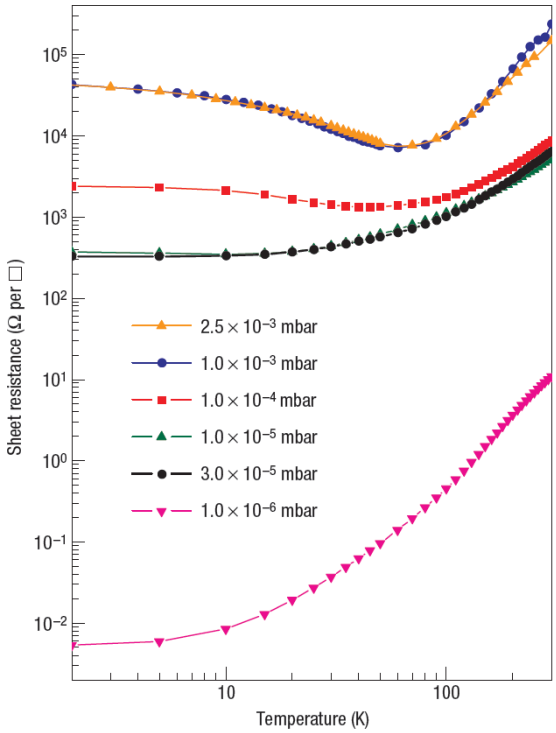

Figure 2.1: Temperature dependence of the sheet resistance for LAO/STO samples grown at several growth pressures. Figure by Brinkman *et al.*[22] Reprinted by permission from Macmillan Publishers Ltd: Nature Materials **6** (7), 493-496, copyright 2007.

Weak localization[23] (an increase in resistance around zero magnetic field, due to localization of electrons) and weak anti-localization[24] (a decrease in resistance around zero magnetic field, see also Chapter 6) have been observed around zero magnetic field. Effects such as universal conductance fluctuations[25, 26] (fluctuations in the conductance due to inhomogeneous scattering centers) have also been observed.

Figure 2.1 from Brinkman *et al.*[22] suggested the growth pressure of the LAO to be the key factor for the temperature dependence of the sheet resistance. The resistivity of the top two curves in figure 2.1 shows metallic behavior upon cooling down from a temperature of 300 K down to 70 K. From 70K to lower temperatures the resistance increases and saturates at the lowest temperatures. This is indicated as a Kondo upturn, which is caused by the alignment of spins.[22]

Also ferromagnetism was observed when the growth pressure was in the order of 10^{-3} mbar. Up to that time all reports on superconductivity used a growth pressure in the order of 10^{-5} or 10^{-4} mbar, followed by a post anneal. So it was suggested that depending on growth pressure, magnetism (at "high" pressure, 10^{-3}-10^{-2} mbar) or superconductivity (at "low" pressure, 10^{-5}-10^{-4} mbar) was induced. It was found later that a growth pressure of 10^{-2} mbar or 10^{-3} mbar (see Refs. [27] [28]) followed by a post anneal in high oxygen pressure also gives rise to superconductivity. However, it has never been proved that a post anneal is crucial for superconductivity. The first report on magnetic effects [22] had been published

in 2007, but it took several years before other groups[29-31] started reporting on magnetism in LAO/STO. The work from Ariando *et al.*[29] in 2011 demonstrates an electronic phase separation in LAO/STO, into ferromagnetic regions and a quasi-2d electron gas. The ferromagnetism extends up to room temperature. The group of Levy[32] demonstrated that magnetic force microscopy (MFM) on LAO/STO does not show magnetic effects at room temperature. However, when they depleted the 2DEG by applying a large negative top-gate voltage, a clear magnetic signal was observed, that disappeared when the gate-voltage was switched off.

Superconductivity appears in LAO/STO samples below a temperature of about 300 mK[33] . Several groups[34, 35] have reported on the manipulation of the superconducting state by applying a back-gate voltage. A negative gate voltage causes carrier depletion and a lower critical temperature (T_C), whereas a positive gate voltage increases T_C. A large negative electric field drives the system into an insulating state[33]. Tunnel spectroscopy on LAO/STO showed that the superconducting gap increases with decreasing carrier density[36]. A gap could be observed up to temperatures exceeding T = 0.5 K, whereas measurements on the electron gas did not show superconductivity (at all) at those low carrier densities. From this observation it has been concluded that a pseudo-gap exists in the underdoped regime of LAO/STO, similar to the pseudo-gap that has been observed in high T_C superconductors. Conductivity at the interface between two insulators is a surprising feature, the fact that the interface between LAO and STO can show superconductivity and magnetism at the same time[30, 31, 37], may be an even bigger surprise, since magnetism is known to counteract superconductivity. Rashba spin orbit coupling (the spin of the electron is coupled to its motion) has been reported first by Caviglia *et al.*[24] and Ben Shalom *et al.*[38] They also showed that this coupling can be influenced by applying a back-gate voltage. Several theory papers[39, 40] have discussed the observed spin orbit coupling as a mechanism to pair magnetism and superconductivity in this material system. This topic will be discussed in more detail in Chapter 6.

2.3 Origin of conductivity between insulators

After introducing the main interesting properties of the LAO/STO system, the question rises whether or not we can explain those phenomena. To start with the conductivity, we should look at the interface at the atomic level. STO consists of layers of SrO and TiO_2, LAO of LaO and AlO_2. Considering the valence of the elements (Sr^{2+}, Ti^{4+}, La^{3+}, Al^{3+}, O^{2-}), the layers carry a charge of SrO^0, $TiO_2{}^0$, LaO^+ and $AlO_2{}^-$. When LAO is grown on STO, and the LaO and AlO_2 layers are considered as simple capacitor-plates, the picture displayed in Fig. 2.2 arises. From these alternating charges an electric field (*E*) can be deduced between the layers. When the fields are integrated over the whole thickness of the LAO, a potential (*V*) across the LAO occurs. This potential diverges with increasing thickness, which is not physical. In order to resolve this diverging potential some kind of reconstruction is needed. This can be either structural (intermixing, oxygen vacancies) or electronic. Each of these reconstructions can also induce conductivity at the interface between the two insulating materials.

The first explanation of the observed interface conductivity was an electronic reconstruction scenario[5, 6]. In Fig. 2.3 it is shown that the diverging potential can be resolved when half an electron per unit cell is transferred from the surface to the interface. For TiO_2 terminated STO, this leads to an excess of ~10^{14}/cm^2 electrons at the interface. The TiO_2/LaO interface can be conducting for several reasons. First $LaTiO_3$ itself can be conducting, even in very thin layers. However, it has been found experimentally that at least 4 u.c. of LAO need to be grown on STO in order to get it conducting[14]. This rules out that the LTO at the interface is the conducting layer. The TiO_2/LaO interface can be conducting due to the valence of Ti. In STO this is Ti^{4+}, however electrons can be added in Ti 3d orbitals, making it Ti^{3+}. When half an electron per unit cell is transferred to the interface, the electrons can occupy the unoccupied d-shell of Ti, leading to a mixture of Ti^{3+} and Ti^{4+} states.

In the case of SrO termination of the STO substrate, a SrO/AlO_2 interface is formed. In this configuration half a hole per u.c. should be transferred to the interface when an electronic reconstruction takes places. However, the costs for removing an electron from the O-2p valence band are too high to make this more favorable than a structural reconstruction. The latter happens in a SrO/AlO_2 interface, where due to intermixing also surface roughening takes place.[6]

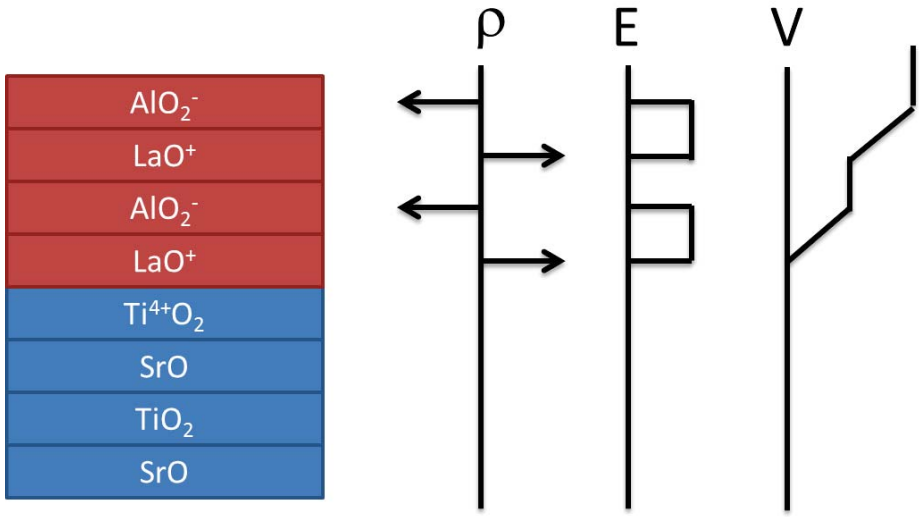

Figure 2.2: Polar catastrophe: the charged layers of LaO and AlO_2 (ρ) lead to an effective electric field (E) across the LAO, leading to a potential (V) across the LAO, that diverges with increasing thickness. Adjusted from Ref[6].

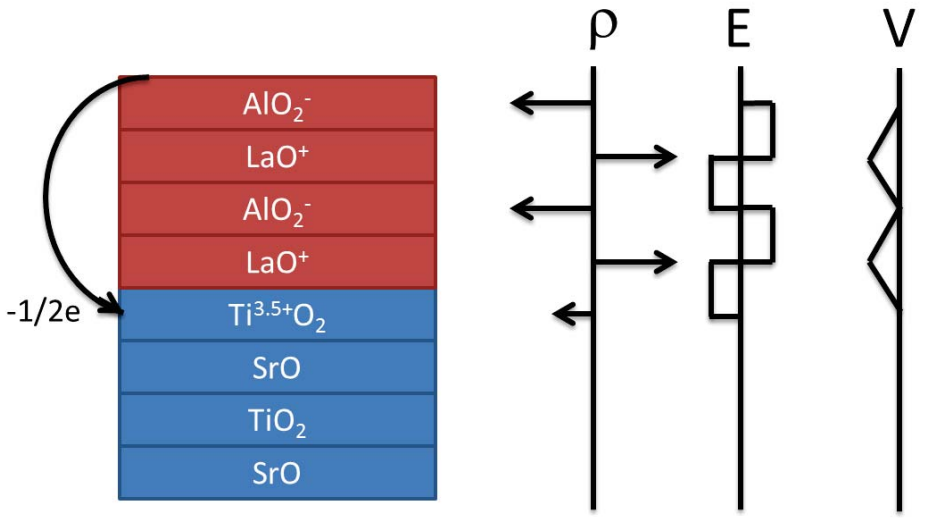

Figure 2.3: Polar catastrophe resolved: by moving half an electron per unit cell from the surface to the interface (in the Ti^{3+} state), the net electric field (E) is zero and the potential (V) does not diverge. Adjusted from Ref[6].

Intermixing of La or Al in STO and/or Sr or Ti in LAO could also lead to a conducting layer, and this has been observed[41]. However, intermixing at the interface alone does not resolve a polar catastrophe. When only a few u.c. show intermixing, the first LaO layer without intermixing, would be the starting point for a new polar catastrophe. Intermixing has to occur in the whole LAO film in order to resolve a polar catastrophe and from TEM studies it has become clear that the interfaces are very sharp, showing little intermixing. This option has to be excluded as reason for the interface conduction.

A third possible reason for conductivity at the interface is the presence of oxygen vacancies in STO. When an oxygen ion is missing from the lattice, this introduces 2 electrons per oxygen vacancy, since the valence of oxygen ions is O^{2-}. In this case the carrier density is enhanced by the introduction of oxygen vacancies. At the same time these vacancies can act as scatter centers when they are located close to the interface, thereby reducing the mobility[16]. Oxygen vacancies can be created in the pulsed laser deposition process when the deposition pressure is low and atoms reach the STO substrate at a high energy. A second potential cause for oxygen vacancies is the fact that the plasma formed when a laser hits the LAO target consists of fractions of LAO, such as La, LaO, Al, AlO etc. Since certain fractions are not fully oxidized when they hit the substrate and have a higher affinity to oxygen then STO, they can extract oxygen from the substrate. This can also explain why STO becomes conducting when amorphous LAO[13] and γ-Al_2O_3[12] is deposited on it.

Oxygen vacancies do not rule out the electronic reconstruction[42]. In fact, oxygen vacancies at the surface of LAO in combination with the electronic reconstruction scenario result in a conducting interface. For this 1 out of 8 oxygen atoms from the top AlO_2 layer needs to be missing. This results in $AlO_{1.75}$, assuming Al to be 3+ and O to be 2-, this leaves a charge of -1/2 electron per u.c. at the surface: exactly the same as in the original electronic reconstruction scenario. The presence of oxygen vacancies at the surface could also be a reason for the extreme surface sensitivity of the system. Prominent examples of surface sensitivity are the increase in mobility to 50,000cm^2/Vs by capping the LAO/STO system with 1 u.c. SrCuO and STO[16], whereas not including a single u.c. STO capping layer results in an insulating sample[43]. Xie *et al.*[18] demonstrate an increase in mobility by using different types of solvents that were put on the sample at room temperature. A decrease in carrier density was reported[17] when $La_{1-x}Sr_xMnO_3$ was deposited on top of LAO/STO, whereas the deposition of $SrMnO_3$ renders the sample insulating[17].

It was found that superconductivity and (ferro)magnetism could co-exist in the LAO/STO 2DEG[30, 31, 37]. Usually these mechanisms counteract each other, so theories had to be developed to explain this. One of the possibilities is that the magnetism and superconductivity are carried by different electrons. Magnetism originates from localized electrons (in the d_{xy} band), as can be deduced from the PFM studies on depleted LAO/STO[32]. Superconductivity can be present in the d_{xz} or d_{yz} band. Those higher energy

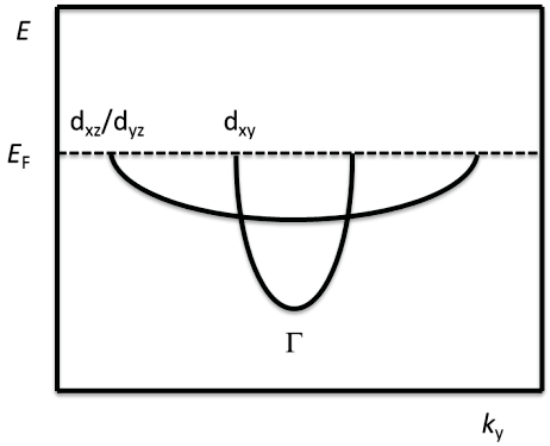

Figure 2.4: Schematic band picture of the conduction bands in LAO/STO. (Figure based on Ref. [44])

bands only fill after the d_{xy} band has been filled. So a certain carrier density is required for superconductivity[45]. And indeed for samples with a carrier density below the Lifshitz transition, that solely have charge carriers in the d_{xy}-band no superconductivity has been observed[16]. In Fig. 2.4 a schematic band picture of the LAO/STO 2DEG near the gamma point is shown. It shows the light d_{xy} and the heavy d_{xz}/d_{yz} bands. Depending on the location of the Fermi level (E_F), one or more bands contribute to the conductivity, magnetism, spin-orbit coupling and/or superconductivity.

2.4 Analysis of the internal electric field using HAXPES

Most of the experimental work in this thesis consists of electrical measurements on the LAO/STO 2DEG. However, there are different techniques that can give insight into the (electrical) properties of the material system. One of these techniques is hard x-ray photoemission spectroscopy (HAXPES). Together with E. Slooten and Prof. M.S. Golden (University of Amsterdam) we measured several samples with a varying LAO thickness ranging from 2-6 u.c. at the Helmholtz Zentrum Berlin. The purpose of this study was to verify whether a potential buildup (as illustrated in fig. 2.2) could be observed, as expected from the polar-catastrophe model, by measuring a shift in the LAO core levels. The observed core level shift (see Fig. 2.5) from 2 to 6 u.c. was ~300 meV[42], smaller than the expected 3.2 eV, however in line with results from tunnel spectroscopy[46]. The discrepancy between the measured and expected core level shift was resolved by suggesting a different reconstruction mechanism. When oxygen vacancies are present at the surface of the LAO, simulations show that the polar catastrophe is resolved and the potential build-up in the LAO is much smaller.

The dependence of the Ti 2p spectrum on the beam energy was also investigated. The higher the beam energy is, the deeper the penetration depth of the electrons is. The Ti 2p

spectrum will change, depending on the ratio between Ti^{3+} and Ti^{4+}, when the system is insulating, only Ti^{3+} states will be occupied, whereas conducting has been linked to the mobile electrons in the Ti^{4+} state. The electron gas is expected to be two-dimensional and should have a finite thickness. Most of the samples did not show a significant difference between measurements conducted at a low or high beam energy, meaning that the thickness of the electron gas extended over 8 nm. However, one sample did show a clear Ti^{4+} signal, that also changed with the x-ray energy, this allowed us to calculate the thickness of the electron gas to be 2.5±1.5 nm.

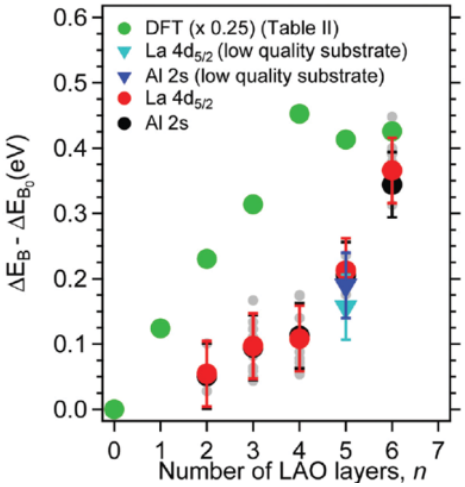

Figure 2.5: Observed energy shift of the La 4d and Al 2s core levels as a function of LAO thickness. Figure from Ref.[42] E. Slooten *et al.* Physical Review B **87** (8), 085128 (2013). Copyright (2013) by the American Physical Society.

2.5 Back-gating and devices

In the previous sections it has been mentioned that certain properties (carrier density, superconductivity, spin-orbit coupling) are tuneable. Tuneable means that the properties can be altered by an electric field, most of the papers discussed above used back-gates to apply the electric field when needed. A clear disadvantage of a back-gate is the fact that it is a global technique. The carrier density in the whole sample is changed, when an electric field is applied from the back-side of the sample. Furthermore, the voltages that need to be used are larger (hundreds of volts), due to the thickness of the STO-substrate. More recently it has been discovered that the tetragonal domains in the STO-substrate start moving when an electric field is applied across it[4]. This movement of the domains causes a change in the conductivity at the surface of the STO (at the interface between LAO and STO). So applying a back-gate voltage changes more than just the carrier density and properties associated with it.

Although back-gating has some serious drawbacks, it has been a successful tool to demonstrate the tunability of properties and also devices. The first device structure in LAO/STO was a transistor-like device, Thiel *et al.*[14] demonstrated that by applying a back-gate voltage, the normally insulating 3 u.c. LAO/STO interface could be switched to conducting. This conducting state was persistent when the back-gate voltage was switched off. Using back-gating, diodes that can operate up to 270 ^{o}C have been reported.[47]

Structured devices in LAO/STO were presented by Schneider *et al.*[48], they reported a technique to define a hard-mask on the STO substrate, this allowed for transport measurements in a Hall-bar configuration (more details about this technique will be discussed in Chapter 3). The Pittsburg group developed a different technique to define nano-structures in LAO/STO[49, 50]. They started with an insulating sample with a LAO thickness of about 3.3 u.c. By using conductive probe atomic force microscopy, they were able to locally polarize the LAO surface. With this technique they were able to sketch devices, such as field effect transistors[40] or nanotransistors that can be operated at gigahertz frequencies.[51]

Capacitance measurements were conducted on LAO/STO samples by Li *et al.*[52]. They fabricated circular YBCO junctions on top of an unstructured LAO/STO interface. By applying a gate voltage, they demonstrated that near depletion, an increase in the capacitance could be observed. This increased capacitance could be related to a negative compressibility of the 2DEG. Later YBCO was also used to define a top-gate[15] that could be operated between - 100^{o}C and + 100^{o}C, it was noticed however, that the apparent carrier density was 90% lower than in un-gated LAO/STO structures. Singh Bhalla *et al.*[46] fabricated circular gold/platinum tunnel electrodes on unstructured LAO/STO. They noticed different tunnel regimes, ranging from direct tunneling (below 8 u.c.) to a region with low tunnel current to a Zener tunneling (above 20 u.c.). Capacitance measurements

on those structures showed hysteresis, indicating a small build-in potential in the LAO of the same order of magnitude as the results discussed in section 2.5.
Hosoda *et al.*[53] reported in 2013 on top-gating of LAO/STO and indicated that the measured dielectric constant of the LAO insulator was smaller than bulk literature values.

As mentioned in Chapter 1, the goal of the work reported in this PhD thesis is to fabricate top-gates on LAO/STO. As will be discussed in the thesis: we were able to fabricate top-gate devices (Chapter 3), tune the conductivity (Chapter 4), superconductivity (Chapter 5) and spin-orbit coupling (Chapter 6) at the interface by using a small top-gate voltage.

Chapter 3

Device fabrication in $LaAlO_3/SrTiO_3$ interfaces

This chapter gives an overview of the fabrication of top-gated LAO/STO devices. It covers structuring of the 2DEG, choice of gate-dielectric and top-gate and all considerations that were made to end up with the final process that delivered working devices.

3.1 Introduction

The physics of the electron gas at the $LaAlO_3/SrTiO_3$ (LAO/STO) interface has shown to be very rich. As described in the previous chapter, magnetism, superconductivity, spin-orbit coupling and many more interesting phenomena occur at this interface. There is an interest in making devices out of LAO/STO interfaces to be able to tune these properties and also because of the fact that the 2DEG is much closer to the surface than in conventional 2DEG systems such as AlGaAs/GaAs. For oxide-2DEGs the interface may be less than 2 nm below the surface[14], whereas for AlGaAs/GaAs the interface usually is more than tens of nanometers away from the surface[54]. The closer proximity of the 2DEG to the surface may result in a more local tunability of the electron gas, or it can lower the required gate voltages.

Figure 3.1. shows a sketch of a conventional field effect transistor (FET). It consists of three main elements, the channel (in light red) between source (S) and drain (D), a gate dielectric (insulator) and the gate itself. Applying a voltage to the gate changes the Fermi level in the channel, allowing for current flow or blocking it. A threshold voltage can be defined as the minimum gate voltage that needs to be applied in order to have a conducting channel between source and drain contacts.

For LAO/STO the threshold voltage strongly depends on the thickness of the LAO. Since in this material system the interface is conducting when the LAO thickness exceeds 4 u.c., instead of insulating for thinner LAO thickness. A first guess would be that a top-gated device with a thickness below 4 u.c. of LAO will have a positive threshold voltage: a positive gate voltage needs to be applied to have conduction at the channel; it does not conduct when no voltage is applied to the gate). Whereas a “thick” sample has a negative threshold voltage: there is conduction at the channel when no gate voltage is applied. However, it is known that adding additional layers on top of the LAO may lower[55] or raise[16] the number of u.c. of LAO required to get a 2DEG, so the choice of gate metal may influence the (sign of the) threshold voltage.

To realize field effect devices in LAO/STO in the form of top-gated Hall-bar structures, three requirements need to be fulfilled. Firstly, the LAO/STO interface needs to be structured in a Hall-bar. Secondly, a high-quality gate insulator is needed to avoid current between top-gate and 2DEG. Thirdly, the gate electrode needs to be deposited on top of the gate dielectric.

This chapter describes the various approaches that have been followed in the device fabrication to end up with a working FET. The structuring of the 2DEG, the search for a good gate dielectric and finally the method for top-gate deposition will each be elaborated on.

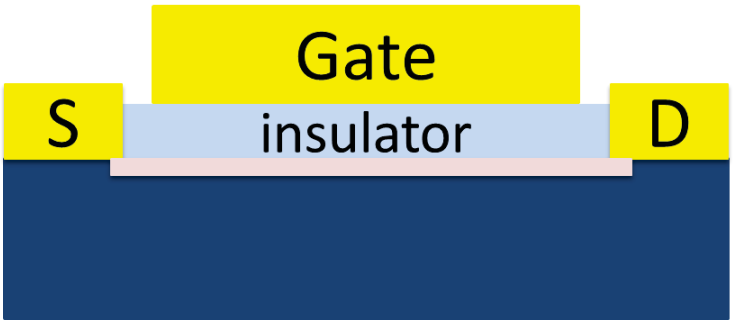

Figure 3.1: Sketch of a FET: Source (S) and drain (D) connected via a conducting channel (light red) on the substrate (dark blue). The channel is separated from the gate by a thin insulator.

3.2 Structuring techniques described in literature

Electronic transport data have been reported since the very first paper on LAO/STO[5]. Othomo and Hwang reported a high mobility electron gas between the insulators LAO and STO. The values for electron density and mobility can be calculated using a Hall-bar or by using a specific geometry, the Van der Pauw[56] method. The first generation papers e.g. Refs.[22, 38, 55] on this topic all used the Van der Pauw setup to calculate these numbers, because this method is simple for the small square LAO/STO samples. The STO substrates have a size of usually 5x5 mm or 10x10 mm, therefore making contacts in the four corners of the sample is sufficient to do a van der Pauw measurement: it does not require structuring of the samples.

To calculate the sheet resistance (which is needed to derive the electron mobility) in the van der Pauw configuration a structure factor is included. This structure factor equals $\pi/ln(2)$ when the measurement is performed on a perfectly square sample, with current and voltage contacts at the corners. A drawback of this measurement method is the fact that in practice contacts are never exactly in the corners and/or the sample is never perfectly square. So there will be a small component in the measured Hall voltage due to the longitudinal resistivity ρ_{xx}. The second disadvantage is that this measurement only gives information about a whole film. These are reasons to use a Hall-bar or a different measurement configuration, which can give more precise values on a more local scale.

A usual way to define a structure in a thin film is by a lift off technique. A photoresist is spun on a substrate and after exposure and development, the material is deposited. After lift off the deposited material has the desired shape on the substrate. This process may be repeated several times to get the final device. Since the LAO layer needs to be deposited at 850 ^{O}C, this is not possible in this material system. The polymer used as resist would simply burn and leave a carbon layer on the substrate. This problem is well known and common in the oxide perovskite material systems. To solve this issue, the films are usually

deposited directly on the substrate and structured by etching. This etching may be physical (using argon ions) or by chemical methods.

For LAO/STO the usual etching methods are non-trivial. There are no reports on successful chemical etching of LAO. It is known that argon ion etching also brings difficulties, since argon ions arrive at a high velocity at the surface of the sample and will penetrate into the STO substrate. In this STO layer, the argon ions create oxygen vacancies. Since each O^{2-} vacancy adds two free electrons to the system, the etched region can easily become conducting.

Several groups developed their own solution to this problem. The solutions range from a post anneal after argon etching[57] or reactive ion etching[58] (using oxygen) to the use of a hard mask[48]. The first report on using a hard mask to define a structure in LAO/STO was made by Schneider *et al.*[48] In that work a structure was defined with photolithography on a 2 u.c. thick film of LAO on STO. The fact that a LAO layer with a thickness below 4 u.c. is insulating[14] was used there. The 2 u.c. of LAO were deposited to not influence the conducting interface between STO and LAO. After this step, amorphous LAO (a-LAO) was deposited. Since this layer is non-crystalline the underlying interface does not become conducting. After lift off, crystalline LAO is deposited at an elevated temperature. After a post anneal at elevated temperature, contacts to the 2DEG were made by ion-milling followed by the deposition of titanium.

The disadvantage of this technique is that the sample gets 2 heat cycles and the sample remains covered by the hard mask consisting of a layer of amorphous LAO. To solve the latter, Banerjee *et al.*[59] developed a technique in which amorphous AlO_x is used to structure the LAO. In their experiments they deposit the AlO_x on the STO substrate and pattern it with photo- or e-beam lithography. The AlO_x can be etched with NaOH and is stable at high temperatures. After LAO deposition the remaining AlO_x can be removed with NaOH, while this leaves the LAO unaffected. This technique leaves a structured LAO film on the STO substrate without any hard mask left on the sample. Using this way of structuring for top-gating can only work when an additional insulating layer is added in order to avoid leakage between top-gate and interface at the edges of the LAO-structure.

3.3 Choice of the gate dielectric

The LAO/STO 2DEG is known to be very sensitive to material on top of the surface of the LAO layer. This is very clear from experiments by the Pittsburgh group where a conducting atomic force microscope (AFM) was used to write conducting lines on a further insulating LAO/STO interface[49]. The interface had 3.3 u.c. of LAO, so it was below the critical thickness of 4 u.c.. It became conducting due to the fact that water, that is always present in a humid environment, splits in H+ and OH- ions at the LAO surface. By applying a positive bias to the tip, the OH- ions were removed from the surfaces, leaving positively charged H+ ions at the surface. These positive charges give an effective field effect and

raise the carrier density at the interface. Experiments in which samples were cleaned by different kinds of solvents also changed the carrier density[18]. Experiments in Twente showed that the critical thickness can be reduced to 1 u.c. of LAO, when a capping layer of 1 u.c. STO was added[55]. Recent work on a multilayer of STO/LAO/$SrCuO_3$/STO showed a critical thickness of 6 u.c. of LAO before the interface became conducting[16]. If the STO capping was not deposited, the STO/LAO/$SrCuO_3$ system was insulating for all tested LAO thicknesses.[43]

Experiments with a stack of STO/ 2 LAO/ 1 STO/ 1 SrO always gave insulating samples. Calculations on adding a SrO capping on a LAO/STO layer confirmed that a SrO capping does not give rise to a 2DEG at the LAO/STO interface.[60]

From all of these examples it is clear that the surface of the LAO plays an important role in the electronic properties of the 2DEG; adding a gate dielectric on top of LAO may change the conductivity of the 2DEG. Therefore the choice of the gate dielectric is important.

3.3.1 Common gate dielectrics

Two commonly used gate dielectrics are SiO_2 and Al_2O_3. Both of these materials can be sputtered or e-beam evaporated. However, both deposition techniques do never deposit a fully oxidized gate dielectric, an oxidation step is needed after deposition. Since Si and Al have a higher affinity to bind oxygen than LAO, it is likely that the LAO would loose some oxygen to an overlying gate dielectric, prior to the oxidation. Oxygen vacancies in the LAO layer may alter the properties of the 2DEG.

Atomic layer deposition or pulsed laser deposition in high oxygen pressure may be options to deposit these dielectrics fully oxidized on the LAO. However, an extra interface will be created between LAO and SiO_2 or Al_2O_3, which may make this system even more complex.

Because of these expected problems when SiO_2 or Al_2O_3 would be deposited, we decided to find for an alternative gate-insulator, which would not have the same issues.

Room	Temperature (^oC)
Furnace	690
Chamber	135
Vaporizer	175

Table 3.1 Parylene coater settings

3.3.2 Parylene

Parylene is a polymer, which is used as a coating for electric circuits, so it should not influence the properties of the materials it is evaporated on. Furthermore, it has a relative high dielectric constant for a polymer (ε_r = 3) and it is stable at low temperatures. Since these properties are exactly what is needed for a gate dielectric, a first attempt to gate the LAO/STO top-gate has been made by depositing parylene C ([i]) on top of a 10 u.c. LAO Hall-bar.

The parylene has been deposited by vapor deposition in a SCS parylene coater. The deposition settings can be found in table 3.1. The temperature of the sample in the deposition chamber was about 25 ^{o}C and the pressure about 25 mbar. In order to ensure good adhesion of the parylene, 1 mL of silane was distributed in the deposition chamber before closing it.

As mentioned in the previous paragraph, it should be investigated what influence the deposition of a material on top of the LAO has on the 2DEG properties. Figure 3.2 shows the temperature dependence of the carrier density and mobility of a Hall-bar structure in 10 u.c. LAO on STO. Prior to parylene deposition a first set of measurements (black squares) has been done. After the deposition of 500 nm parylene and gold top-gate sputtering, for this specific device the top-gate and 2DEG were accidentally shorted. Therefore the parylene and gate have been removed by etching it in HNO_3 (69%). After parylene removal, the carrier density and mobility (gray circles) showed values comparable to the measured sample before parylene deposition. From this we can conclude that the deposition and removal of parylene does not influence the 2DEG properties.

For gating, a high electric field is necessary. To get a high electric field, a high potential across a thin dielectric with high dielectric constant should be applied. For this purpose a relatively thin layer of 50 nm of parylene has been deposited on a 10 u.c. LAO/STO Hall-bar. After this photoresist is applied to structure a top-gate has been deposited by sputtering and lift off of gold.

The leakage current at T = 2K has been measured and is displayed in Fig. 3.3. Compared to the measurement current of 1 μA, the leakage current I_G is small for V_G between -18 V and +45 V (< 12 nA).

The resistance R in the 2DEG as function of gate voltage is displayed in Fig. 3.4. It shows that applying a negative gate voltage increases the resistance, whereas a positive gate voltage leads to a lower resistance. The figure has been measured after several gate sweeps that were needed to get a fixed resistance at a specific gate voltage that did not change as a function of time, what did happen when the gate voltage was applied for the

[i] Parylene C = poly (para-xylylene) with one of the aromatic hydrogens replaced by a chlorine atom.

first time. In Fig. 3.4 an increase in resistance is observed at V_G < -18 V. From Fig. 3.3 has been observed that at this gate voltage, the gate current rapidly increases. This current influences the measurement current and therefore the measured sudden increase in the resistance is a measurement artifact. For a positive gate voltage a similar effect appears around V_G > 40 V.

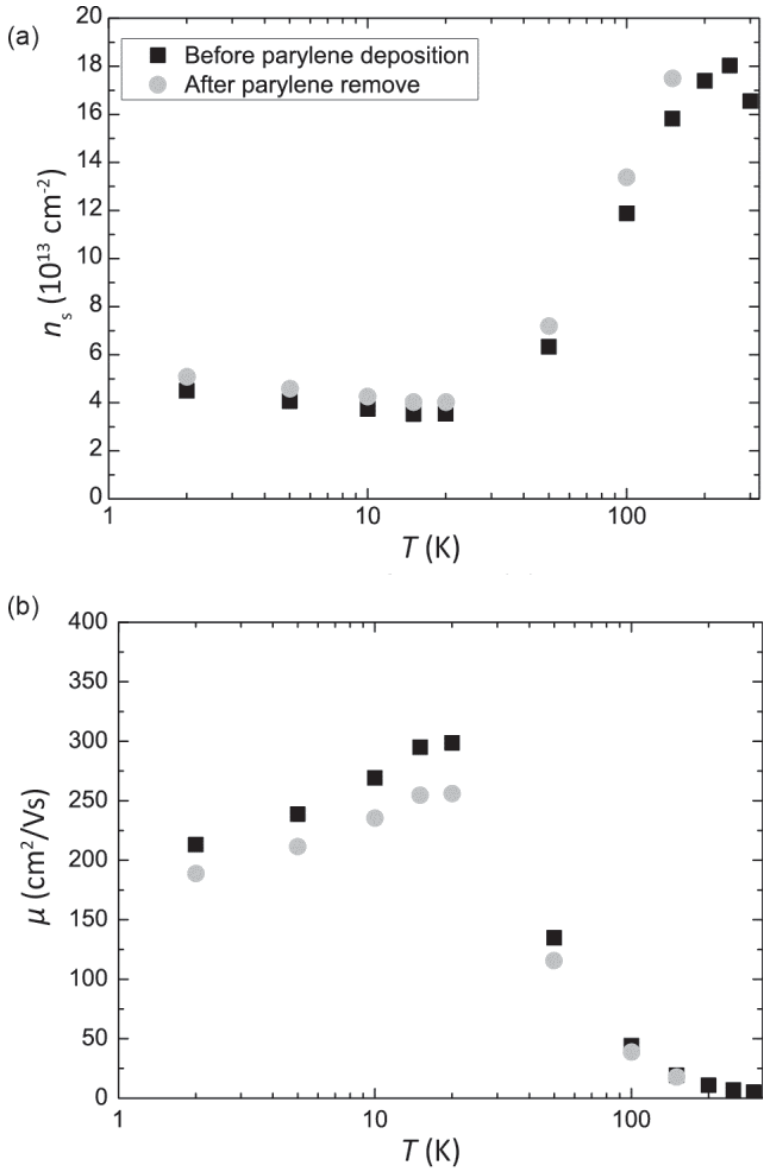

Figure 3.2: Temperature dependence of the carrier density (a) and mobility (b) for a single Hall-bar, measured before the deposition of parylene (black squares) and after (gray circles) the removal of the parylene.

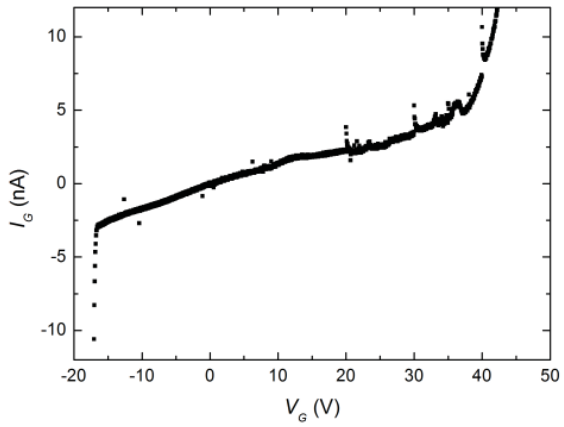

Figure 3.3: Gate current as a function of gate voltage at 2K. Measured on a 10 u.c. LAO Hall-bar covered with 50nm parylene with sputtered gold electrodes.

To check the stability of the system, the longitudinal resistance (R) measured in the Hall-bar structure at a fixed source-drain current has been measured, while the gate voltage V_G is switched between on and off. This is displayed in Fig. 3.5. In this figure in black the measured longitudinal resistance R is shown on the left y-axis. On the right y-axis the applied V_G is shown. The figure shows that applying a large negative gate voltage, V_G = -30 V increases R from 4.3 kΩ to 5.3 kΩ. When V_G has been switched back to 0, the stable resistance has increased to 4.6 kΩ. After this initial setting at V_G = -30 V, the resistance recovers when switching V_G from on to off for -25 V < V_G < 35 V. Increasing V_G > 40 V, the resistance does not stabilize anymore, as can be seen from the steady decrease in resistance as function of time, Furthermore, the resistance does not recover to its original value, but remains lower. Even pulses as big as -30 V, that were used to set the system at the beginning of the measurement are not enough to bring the system in a stable configuration.

From Figs. 3.4 and 3.5 we conclude that when a positive voltage bigger than the breakthrough voltage (the voltage at which the gate current rapidly increases) is applied to the top-gate, the longitudinal resistance of the Hall-bar decreases. Even when the gate voltage is decreased to 0, the resistance of the Hall-bar does not recover to its original value.

A possible explanation is that current flows through the parylene and electrons get trapped. These trapped electrons create a local electric field and this modulates the conductivity of the 2DEG through the field effect.

After a gate sweep, at V_G = 0 V a local electric field is present. This will lead to a lower resistance in the 2DEG. If this is the case, the resistance should increase as a function of time until all possible traps are filled with (immobile) electrons.

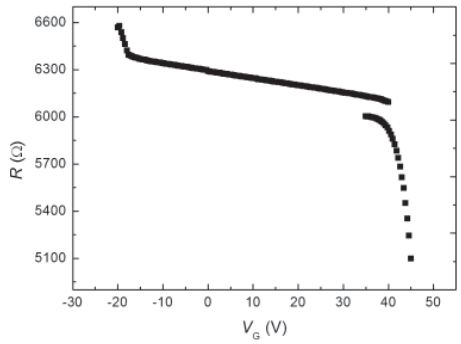

Figure 3.4: Resistance at *T* = 2K as function of gate voltage for a 10 u.c. STO/LAO Hall-bar with parylene gate dielectric.

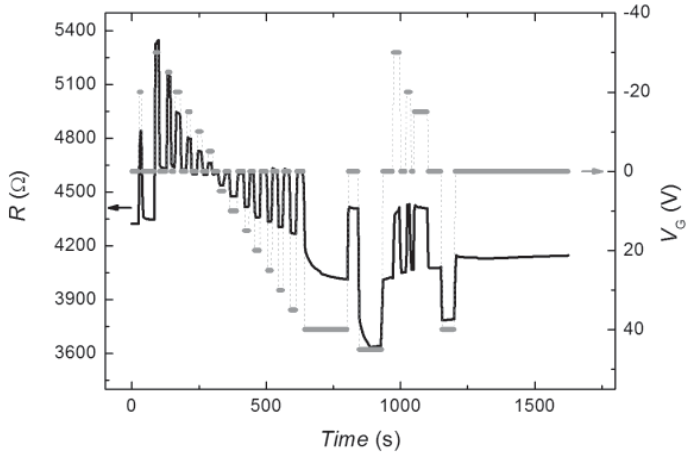

Figure 3.5: Resistance (black) as a function of time for different gate voltages (grey circles). Measurement at *T* = 2K on a 10 u.c. STO/LAO Hall-bar with parylene gate dielectric.

3.3.3 $LaAlO_3$ as gate insulator

Since parylene (on top of LAO) as a gate dielectric shows a leakage current comparable to the measurement current, when the longitudinal resistance only changes by 10%, a different gate dielectric is preferred. As discussed in section 3.3.1 common dielectrics Al_2O_3 and SiO_2 may create oxygen vacancies in the LAO layer and additional interfaces between the LAO and dielectric. Other oxide perovskites like $SrTiO_3$ and $SrCuO_3$ are known to alter the 2DEG properties. On the other hand, bulk LAO itself is known to be a high k-dielectric with a dielectric constant $\varepsilon_r = 25$ at room temperature[61]. Since the 2DEG at the STO/LAO interface occurs due to the presence of the LAO layer, a choice for LAO as gate dielectric would be natural.

The choice for LAO as gate dielectric limits the insulator thickness to a maximum of about 10 nm, since the LAO film will peel off the substrate when its thickness exceeds 26 u.c.[62].

Due to this limited thickness of the insulator, the metal for the gate electrode should not penetrate into the insulator when deposited in order to avoid large gate current.
The minimum thickness of the gate insulator is determined by the critical thickness of LAO for conductivity, since a thinner layer would not give rise to a conducting interface. A FET that does not conduct at zero gate voltage (with a positive threshold voltage) would require a LAO thickness below the critical thickness. However, difficulties can be expected in the design, since a conducting path between source and drain would require the whole structure to be covered by a top-gate. Furthermore the gate current is expected to be large, since the distance between 2DEG and top-gate is very small (<1.2 nm in case of a critical thickness of 4 u.c.).
We choose to work with LAO with a minimum thickness that exceeds the critical thickness, so that is conducting when no gate voltage is applied.

3.4 Top-electrode deposition and definition

As discussed before, the materials on top of the LAO can influence the properties at the LAO/STO interface. Therefore, the choice of the metal for the top-gate is non-trivial. To avoid the creation of oxygen vacancies at the LAO/gate interface, we decided not to use metals that easily oxidize, such as aluminum, titanium or niobium. For our purpose a noble metal would be perfect, we choose gold as metal for the top-gate. Any other noble metal acting as top-gate could be interesting for further study.
Usually an adhesion layer of chromium or titanium is applied prior to gold deposition. Since an adhesion metal forms chemical bonds with the insulator, this may influence the properties of the LAO. To avoid additional influences of this layer, we also choose not to use an adhesion metal.
Sputtering is a common technique to deposit gold. However, this technique is quite invasive as atoms arrive at the surface with high energy and easily penetrate a few nm in the material. For experiments conducted in Twente, sputtering a top layer of gold on top of LAO/STO always led to an Ohmic or Schottky like contact to the 2DEG.
A crucial step in enabling top-gating in LAO/STO in the work discussed here, has been the use of e-beam evaporation. Gold top-gates have been deposited using this deposition technique at a rate of 0.02 nm/s for the first 20 nm and at a rate of 0.1 nm/s for the last 80 nm. The slow growth rate and soft deposition technique enabled high quality top-gates, as will become clear in the next chapters, where the room temperature properties of LAO as gate insulator will be discussed in chapter 4 and low temperature data will be covered in chapter 5.

3.5 Structuring of the 2DEG

3.5.1 Substrate preparation

To obtain a conducting electron gas at the interface between $SrTiO_3$ and $LaAlO_3$, a single terminated (TiO_2) surface is needed. Commercially bought STO substrates standardly have a mixed termination; a part of the surface is covered by SrO and a part by TiO_2. In order to remove the SrO and to get a single terminated surface a procedure has been developed by Koster *et al.*[63] The slightly modified process that has been used for the STO substrates that were used in this work will be explained in detail in Appendix B.1.

3.5.2 Pulsed laser deposition

LAO is deposited by pulsed laser deposition (PLD). A mask is used to select the most uniform part of the light of a KrF laser, which is focused by lenses at a single-crystalline target of LAO. Before deposition, the target is grinded with sandpaper to make sure that the target is clean to avoid cross contamination. This target is placed (via a load lock) inside a vacuum system with a background pressure of about $2x10^{-7}$ mbar. Facing the LAO target is a heater on which a singly terminated STO substrate is placed.

The backside of the substrate is glued with conducting silver paint to the heater. The amount of silver glue is crucial for a good thermal connection between heater and sample. If too much glue is applied, it may form a droplet underneath the sample. When the sample is then pressed to the heater, the silver paint may cover (a part of) the polished side of the substrate. If not enough paint is applied, the sample may fall off, or the thermal connection may be not uniform, leading to a non-uniform film. This is clearly visible when the sample is at deposition temperature, since the whole sample should be glowing in a uniform red color. If there are darker parts visible, these parts are colder and insufficient paint has been used. At room temperature a shutter is placed between the target and the sample and the moving target is pre-ablated (in such a way that each segment of the target is scanned four times) at a repetition frequency of 5 Hz to avoid any contamination during deposition. The shutter is now removed and the sample is aligned to the Reflection High Energy Electron Diffraction (RHEED) beam.

The sample is heated up to deposition temperature (in general 850 ^{o}C) in the deposition pressure (in general 2×10^{-3} mbar oxygen). The RHEED alignment is adjusted a little bit to compensate the expansion of the substrate and heater at these elevated temperatures. The intensity of the (001) main reflection of the STO substrate is measured and recorded during the LAO deposition and will oscillate. A maximum in the intensity of the reflection relates to a smooth surface, where a minimum is connected to a half filled surface. The period of one oscillation is therefore the time needed to grow one unit cell of LAO. By counting the number of oscillations, the layer thickness can be determined. The

deposition is stopped at a maximum to make sure that the top layer is completely finished. The sample is then cooled down in the deposition pressure at a rate of 10 ^{o}C/min and removed below a temperature of 75 ^{o}C from the system.

3.5.3 Structuring

If one wants to do measurements in a configuration different from the van der Pauw configuration, the film has to be structured. (Due to the fact that the samples are square, for a van der Pauw measurement no structuring is needed.) At the starting point of this work, the method described by Schneider *et al.* [48] was the most promising candidate to structure the LAO/STO interface. This process (as has been described in section 3.2) involves applying a hard mask of a-LAO after the deposition of 2 u.c. crystalline LAO on STO. It also requires two cycles of heating up and cooling down the sample. We tried to reduce this to one heating cycle, by using the same structuring technique directly on the STO substrate, without depositing first 2 layers of LAO. Here the process flow will be discussed, for more details see Appendix B.2.

Figure 3.6 shows the process flow for making a top-gated LAO/STO sample. First a single terminated STO substrate is needed (a), on this substrate photoresist is spun (b) and structured in alignment markers (c), a-LAO is deposited at a thickness of 100 nm for alignment markers. This thickness is needed because a-LAO is transparent and a thinner film does not give enough optical resolution for alignment of further lithography steps. After deposition the photoresist is removed by ultra-sonication in acetone (d). Steps (b-d) are repeated to deposit the actual hard-mask of a-LAO. For the second deposition, the thickness of the a-LAO needs to be thinner, 10 nm, in order to avoid conductivity at the STO/a-LAO interface.

Crystalline LAO can be deposited (e) after removing the photoresist from the a-LAO deposition. After deposition, a post-anneal in oxygen is included to remove the conductivity at the STO/a-LAO interface. After this step photoresist is applied (f) and titanium/gold (bond) contacts to the 2DEG and on the a-LAO (g) (for bonding to the top-electrode) are sputter deposited. The last photolithography step (h) is needed to define the top-gate structures, that are deposited by e-beam evaporation (i). Figure 3.7 shows the final devices.

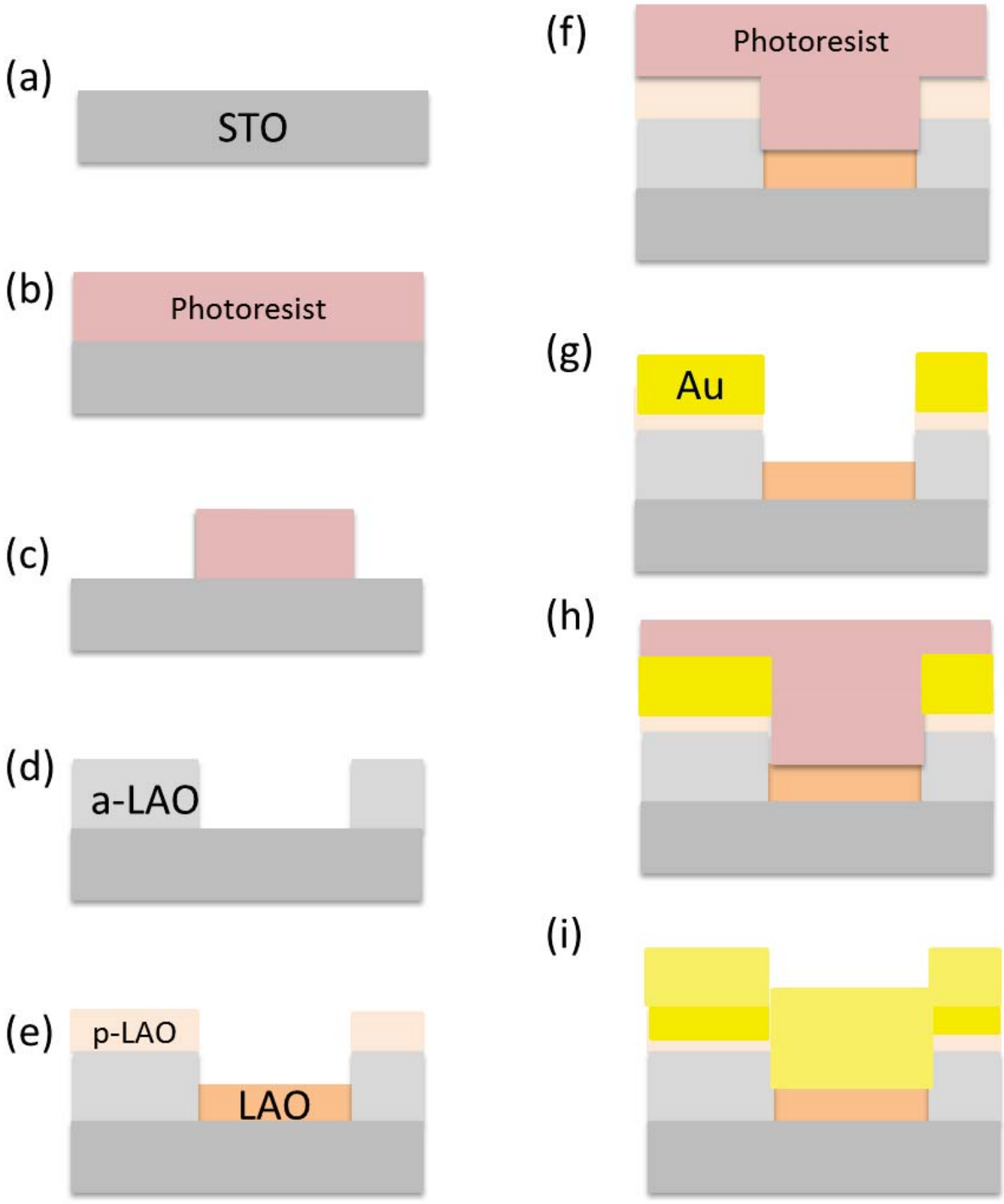

Figure 3.6: Schematic overview of device preparation (a) Single terminated STO substrate (b) photoresist applied at bare substrate (c) Photoresist developed (d) amorphous LAO deposition at room temperature (e) crystalline LAO deposition. LAO on top of a-LAO will be polycrystalline (p-LAO) and the interface insulating (f) photoresist applied (g) gold contactpads deposited via sputter deposition (h) photoresist applied (i) gold top-gates evaporated, in order to avoid shorts to the 2DEG.

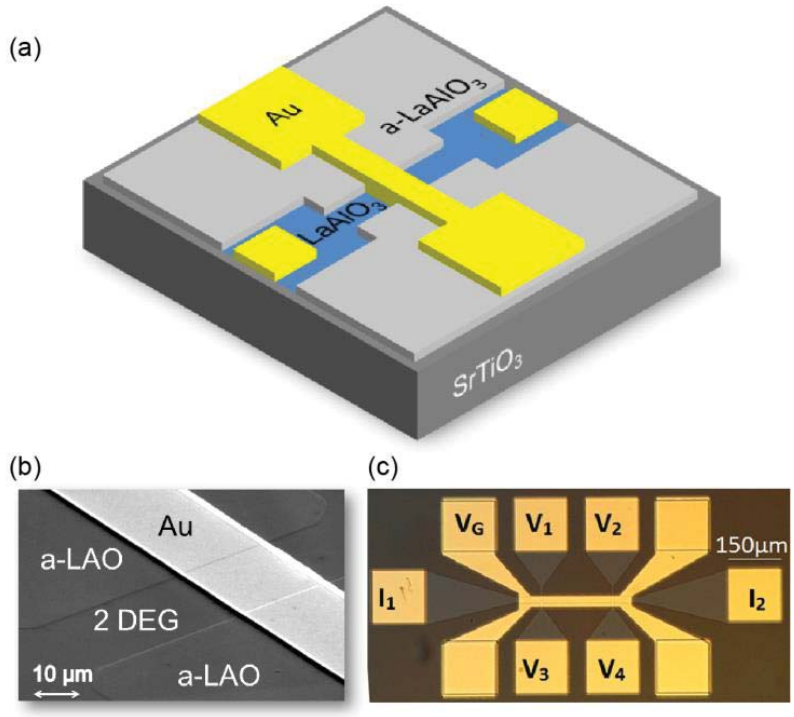

Figure 3.7: (a) schematic of a cross-bar junction. (b) Scanning Electron Micrograph of a cross-bar junction. (c) Optical image of a Hall-bar in LAO/STO with a golden top-gate. The dark area is insulating a-LAO, the light gray area is conducting LAO/STO, the squares are sputtered gold, whereas the top-gate is made of e-beam evaporated gold.

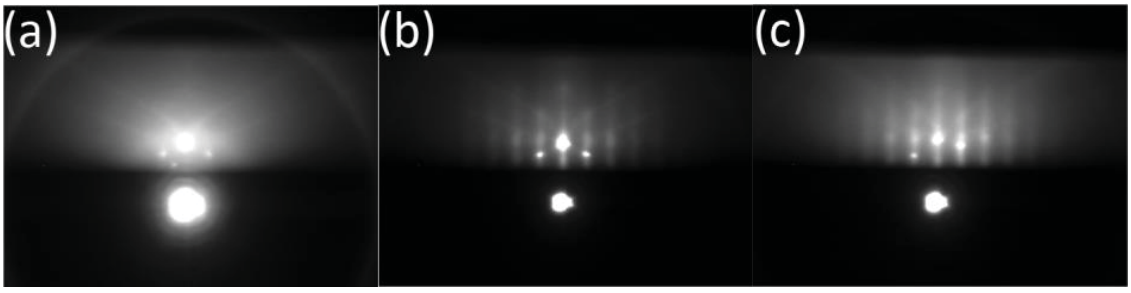

Figure 3.8: RHEED images of a deposition with a structured substrate. (a) STO substrate with a-LAO (at 120 ^{o}C) (b) STO substrate with a-LAO (at 850 ^{o}C) (c) after deposition of 5 u.c. of LAO (at 850 ^{o}C).

3.5.4 RHEED

To be able to see a RHEED reflection when using small structures, the mask is designed to have a 1x1 mm square in the middle of the sample that is not covered by a-LAO. The RHEED should be aligned to this region. When most of the substrate is covered by a-LAO the RHEED alignment should be done at room temperature, in the deposition pressure. This alignment needs to be done at room temperature, because the a-LAO starts to crystallize above 750 ^{o}C and the difference between STO substrate reflection and a-LAO reflections is not visible anymore, see Fig 3.8(b). At room temperature the STO substrate reflection will be visible (see Fig. 3.8(a)) and this spot has to be monitored during heating the sample (in this way one can select the correct spot for monitoring the growth when the system is at deposition temperature). The blur that is visible in this image, is caused by the a-LAO that scatters the electrons.

3.5.5 Electrical characterization

For a thin film of LAO/STO measured at T = 2 K, in the Van der Pauw configuration or in a Hall-bar setup the carrier density (n_s) is comparable , the typical n_s = 2 x 10^{13} cm^{-2}. However, the typical electron mobility (μ) typically differs between the two measurement setups. For a typical sample measured at T = 2 K, in the Van der Pauw configuration, μ = 1000 cm^2/Vs. Whereas for a typical sample measured in the Hall-bar setup μ = 400 cm^2/Vs. The different way of processing the sample may cause this difference in mobility. The Hall-bar samples have been covered with photo resist directly on the STO, although the cleaning has been done carefully, a very thin layer of resist may remain. When this layer burns at elevated temperatures, carbon particles may degrade the LAO/STO interface quality.

The hypothesis that the difference in mobility determined via the van der Pauw method (on the whole sample) or the (much smaller) Hall-measurement, can be explained by the fact that the van der Pauw method is a global technique, whereas the Hall-measurement is a more local technique, with possibly more defects and thus a lower mobility, can be falsified. Since one would expect more variation in the local Hall-measurements and incidentally measure a very high mobility, and we have not observed this variation in mobility for Hall-bars on the substrate.

To find the exact reason for the observed difference in mobility a more specific study on this topic is needed.

3.6 Conclusion

In this chapter the road towards successful fabrication of Hall-bar structures in LAO/STO with a top-gate has been discussed. For the Hall-bar fabrication the inclusion of a post-

anneal in high oxygen pressure after the growth of crystalline LAO was necessary. Why these Hall-bars have a lower mobility then bare films is still an open question. In order to influence the conductivity of the Hall-bar a top-gate was added on top of it. As an insulator between the Hall-bar and the top-gate a first choice was made for parylene. The (gate-leakage) properties of these devices were insufficient to continue research with parylene as the gate dielectric, since the gate-current was comparable with the measurement current before a significant effect of the electric field on the 2DEG was observed. A next round of experiments was conducted on samples without an additional dielectric, since LAO is a dielectric itself. The key improvement in sample fabrication was the choice to use e-beam evaporation for the deposition of the gold top-gate electrode.

A suggestion for further research on the fabrication process is the use of different growth pressures for the crystalline LAO deposition. The pressure used in the work described in this thesis is quite high (2×10^{-3} mbar), whereas other research groups use a deposition pressure of 10^{-5} mbar to 10^{-4} mbar. It may be interesting to investigate whether or not the gate current through the LAO depends on the growth pressure of LAO.

A second suggestion is to use different metals as a top-gate and investigate their influence on the transport properties in the 2DEG and their influence on the leakage current.

The third suggestion is to deposit a top-gate on a high mobility sample, such as the STO/LAO/$SrCuO_3$/STO system. A further advantage of the use of this material system is the fact the intrinsic carrier density is about an order of magnitude lower, so a much smaller electric field should be needed to observe changes in the conductivity of the 2DEG.

Chapter 4

Top-gating of the LAO/STO 2DEG at room temperature

This chapter covers top-gating at room temperature. It focusses on the tunnel current, where aspects as thickness, temperature and pressure dependence will be discussed. Depletion and enhancement of the carrier density in the 2DEG due to an applied electric field are demonstrated.

4.1 Introduction

A lot of focus has been on the physics in the LAO/STO at low temperatures, since the mobility of the electron gas is much higher (3 to 4 orders of magnitude) at T = 2 K than at room temperature. However, the properties of LAO/STO devices at room temperature should also be studied, as commercialization almost always requires room-temperature operation of devices. Potential applications as a gas sensor, for example, where the surface sensitivity plays a key role, urge for a proper understanding of the system properties at room temperature. Even slightly elevated temperatures (although not discussed here) may be very interesting. For a good understanding of the material properties, it is necessary to investigate how oxygen diffusion at elevated temperatures changes the properties of devices. It raises the question whether or not it is possible to make an oxide transistor, that operates at high temperatures where conventional silicon-based transistors fail?

In this chapter room-temperature electron transport measurements on LAO/STO devices will be discussed. The measurement setup will be briefly discussed in section 4.2. Section 4.3 will cover gate current, which should be low when the top-electrode acts as a top-gate, but may also give interesting information on the 2DEG properties when it acts as a local probe for tunnel studies. Furthermore, temperature and pressure dependence will be addressed in section 4.4. In section 4.5 the response of the 2DEG conductivity on the top-gate voltage will be discussed. The last section 4.6 covers mobility and carrier density, deduced from $I(V)$ curves.

4.2 Measurement setup

The devices discussed in this chapter are all prepared by the methods discussed in Chapter 3. The top-gate has been prepared by e-beam evaporation of the gold electrode, without any adhesion layer. In this chapter two different kinds of devices will be discussed, which can be discriminated by their top-gate area. Here, the area of the device is defined as the area where the 2DEG is covered by the top-gate. The two devices are classified as small area devices (< 2000 μm^2), where a small gold strip acts as a local top-gate, on a restriction in the 2DEG, as sketched in Fig. 3.7(a) and large area devices (>100,000 μm^2), that have been measured on a Hall-bar device, as displayed in Fig. 3.7(c).

The measurements on the small-area devices described in this chapter in section 4.3, 4.4 and 4.5 have been performed in a low-temperature probe station. Unless otherwise stated, the measurements have been performed in ambient pressure and at room temperature. In order not to damage the bond pads, copper coated probes have been used to contact them. To avoid influence of photo-activated carriers, after connecting the probes to the bond-pads, the window of the probe station has been covered with a metal

blank. Since the probe station only has 4 probes and 1 probe is needed to connect to the top-gate, the *I(V)*-measurements on the 2DEG have been performed in a 2-point configuration. The typical setup is displayed in Fig. 4.1. Two Keithley 2400 Source Measure Units (SMU's) have been used. One SMU sources a source drain voltage (V_{SD}) and measures the resulting source drain current (I_{SD}). The second SMU has been used to apply a gate voltage (V_G) and to measure the corresponding gate current (I_G). V_G has been applied to the top-gate, relative to the 2DEG, by placing the tip corresponding to the positive side of the SMU which supplies the gate voltage on the bond pad linked to the top-gate. The negative electrode has been linked to the negative electrode of the SMU supplying V_{SD}, which is connected to one side of the 2DEG. One of the possible complications of a 2-point configuration is the contact resistance between the contact pads and the 2DEG if this is not Ohmic. From the linear *I*(*V*)-curves in Fig. 4.3(b) we can conclude that this is not an issue in the measurements discussed here.

The measurements described in section 4.6 have been conducted on a Hall-bar device, as displayed in Fig. 3.7(c). These measurements have been performed after the sample has been glued to a puck to enable measurements at low temperature. The sample holder has been placed in a closed metal box connected to the Delft Electronics measurement setup. The measurements have been performed by applying I_{SD} between I_1 and I_2 (see Fig. 3.7(c)) and measuring the corresponding voltage drop V_{SD} between V_1 and V_2. A gate voltage V_G has been supplied by a voltage source to V_G. I_2 and the negative side of the V_G source have been connected to a common ground.

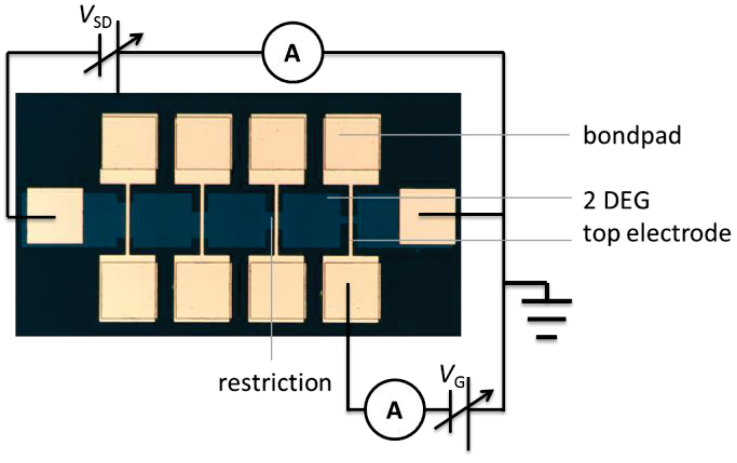

Figure 4.1: Measurement setup for the small-area devices. V_G is applied to one of the 4 small gold strips covering a restriction in the 2DEG. V_{SD} is applied to the 2DEG. The negative electrodes of V_G and V_{SD} have been linked together and to ground.

4.3 Room temperature measurements of the gate current

4.3.1 Low gate current

The key purpose of a gate dielectric is that it should electrically insulate the metal top-gate from the conducting channel underneath. However, when a sufficiently large voltage is applied to the top-gate, the insulator will break down and a gate current I_G starts flowing. The maximum voltage that can be applied to the top-gate before breakdown depends on the material properties of the gate dielectric, including the actual material choice. However, also stoichiometry and quality of the material play a role, just as the insulator thickness.

Sing Bhalla *et al.*[64] conducted measurements on evaporated electrodes on LAO/STO. They investigated the dependence of the tunnel current on the thickness of the LAO insulator. They could discriminate three regimes: at a thin LAO thickness (less than 8 u.c.) direct tunneling takes place between the top electrode and the 2DEG; at a thick LAO thickness (more than 18 u.c.) Zener tunneling takes place. The intermediate region (between 8 and 18 u.c.) shows a low tunnel current. In this section we focus on measurements on an 11 u.c. LAO sample, so our sample is expected to be in the low tunnel current regime.

Figure 4.2 shows the gate current of a small area device (500 μm^2) as function of gate voltage, measured at room temperature. From this figure it can be concluded that up to V_G = 0.5 V the gate current is very small: $I_G < 1$ nA. Upon increasing V_G to higher gate voltages, a significant gate current starts flowing. For negative V_G ($V_G < 0$), the gate current increases to about 1 nA at V_G= -2 V as indicated in the figure. The gate voltage can be increased further down to a maximum tested voltage V_G = -200 V, without an increase in I_G ($I_G < 1$ nA for all tested $V_G < 0$ V).

In order to explain the fact that the gate voltage can be increased to such a high value without a significant gate current, one should have a look at Fig. 4.3(a) where the source drain current I_{SD} is plotted as function of V_G. From this figure it is clear that for $V_G < -0.8$ V the conducting channel is depleted completely ($I_{SD} = 0$). Also from the almost zero slope for the V_G = -1V curve in Fig. 4.3(b) it can be concluded that the resistance of the 2DEG is very high. If there would be any defect in the insulating LAO layer, through which current from the top-gate to the 2DEG could leak, this would not lead to a gate current, since the 2DEG itself has been depleted and does no longer conduct. The area where leakage occurs is therefore greatly reduced, to only the corners of the top-gate. The only possibility for leakage (once the 2DEG is depleted) would be from the top-gate to the leads, since these leads are not covered by a gate and therefore harder to modulate by the electric field. However, since the 2DEG has been depleted, the electric field will be focused, and thus stronger near the corners. This could lead to a local depletion in the leads, which could reduce the leakage even further.

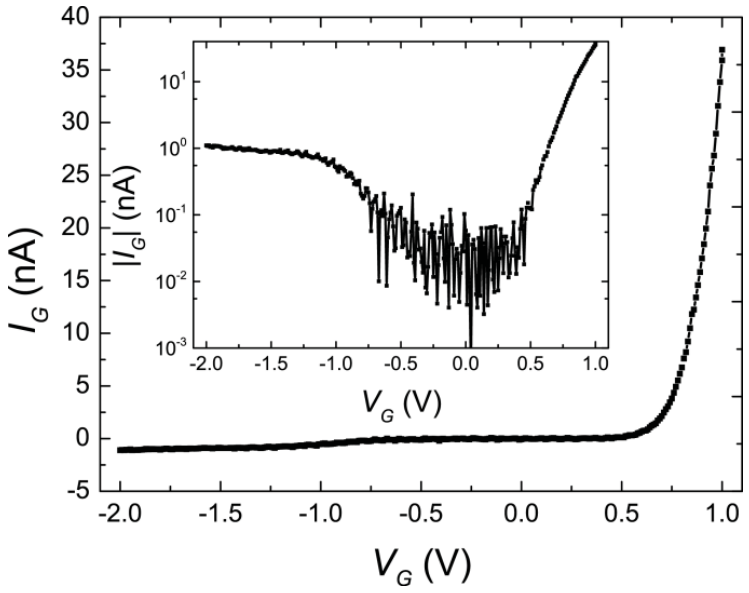

Figure 4.2: Gate current as function of V_G for an 11 u.c. film with an area of 500 µm^2, measured at room temperature. The inset shows the data on a logarithmic scale.

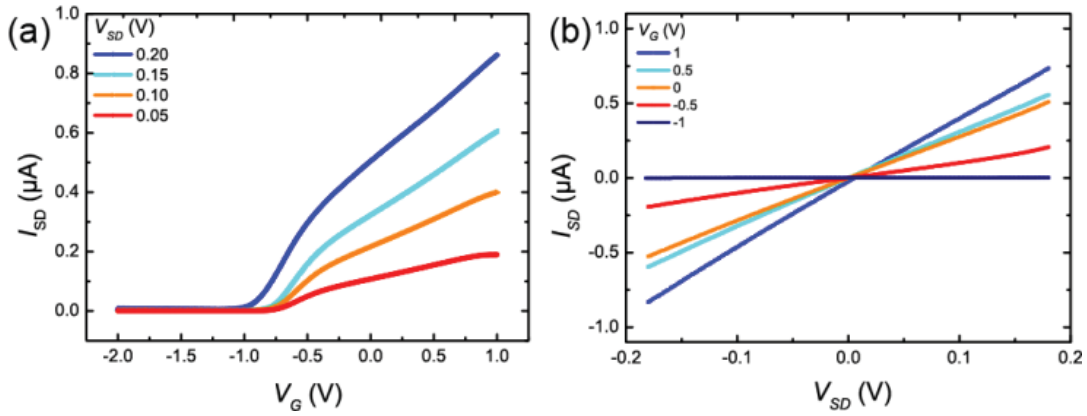

Figure 4.3: (a) Drain-source current I_{SD} as a function of top-gate voltage for source-drain voltages of 50, 100, 150 and 200 mV for an 11 u.c. LAO cross-bar structure with a gate area of 500 µm^2. (b) I_{SD} (V_{SD}) curves of the same structure for top-gate voltages of -1, -0.5, 0, 0.5 and 1 V. Both measurements have been performed at room temperature.

4.3.2 High gate current

When a thin dielectric is used, direct tunneling may be possible between the top-electrode and the 2DEG[64], whereas this is negligibly small for thicker insulator thicknesses. Second to that the gate current should depend exponentially on the thickness of the insulator. Therefore a device with a thinner insulating barrier is expected to carry a higher gate current.

Figure 4.4 shows I_G as a function of V_G for a small device of 500 μm^2 for samples of thicknesses of 5, 11 and 16 u.c., which correspond to 1.9, 4.1 and 6.0 nm, respectively. V_G has been swept and the corresponding I_G has been measured. The arrows in this figure indicate the sweeping direction. For positive V_G (V_G > 0 V) the gate current I_G shows hysteresis, for the 11 and 16 u.c. devices the gate current is larger upon increasing V_G, whereas for the 5 u.c. device I_G is smaller upon increasing V_G. The difference in hysteresis can be explained by the difference in tunneling mechanisms for the 5 and 11/16 u.c. samples. For the 5 u.c. sample direct tunneling is possible, so the closer the 2DEG is to the interface, the higher the tunnel current will be. Applying a positive gate voltage attracts electrons and thereby decreases the distance between gate and 2DEG. Depending on the sweep direction, the distance between gate and 2DEG is larger (increasing V_G) or smaller (decreasing V_G) and the resulting gate current is smaller (increasing V_G) or larger (decreasing V_G). For the 11 and 16 u.c. devices direct tunneling is not possible due to the distance between gate and 2DEG, therefore the tunneling mechanism has to be different. The observed behavior of a higher gate current upon increasing V_G can be explained when a multi-step tunneling process is assumed, for instance, via oxygen vacancies, as commonly observed in similarly produced perovskites. The movement of these vacancies is relative slow, so the measurements have not been conducted in a steady state. For these samples the oxygen vacancies are the key element for tunneling, a positive gate voltage pushes away the oxygen vacancies that are also positively charged. Vacancies in the LAO layer will have a more uniform distribution at V_G = 0 V and will be located more towards the 2DEG when V_G > 0 V. Therefore, sweeping the gate voltage from a positive value to zero results in a lower gate current than sweeping from zero to positive values.

For negative V_G the 11 u.c. and 16 u.c. LAO devices do not show any gate current, as expected. The 5 u.c. sample does show a gate current for negative V_G, since the gate dielectric has a thickness of less than 2 nm, tunneling may be possible.

The surprising behavior appears when one has a look at the shape of the 5 u.c. curve at V_G < 0 V. I_G increases, has a maximum and decreases. The decrease in gate current with increasing V_G can be seen as a negative differential resistance (NDR). Upon sweeping V_G back from -2 V to 0 V, again a maximum in I_G is observed. The reason for this behavior is the same as discussed before: increasing gate voltage depletes the underlying 2DEG, therefore gate current decreases. Upon decreasing the gate voltage, the conductivity reappears slowly in the 2DEG, leading to a lower I_G compared to the I_G when increasing V_G.

From this figure it seems that the 11 and 16 u.c. sample do not show a NDR in the gate current. However, the current is so low that it is close to the limits of the setup. To see if the NDR also appears in these devices, a higher gate current is needed. Therefore, a larger area device has been measured, since the gate current should linearly depend on the area. Furthermore, averaging over more measurements should decrease instrument noise. Figure 4.5 shows an I_G (V_G) for a 11 u.c. (Hall-bar) structure with an area of 117.000 µm^2 that has been achieved by averaging 201 I_G (V_G) measurements on the same Hall-bar to reduce the statistical error. From this figure it is clear that a similar type of hysteresis appears as in the 5 u.c. sample displayed in Fig. 4.4 since I_G shows a maximum upon increasing V_G ($V_{G\ UP}$) to more negative values and I_G is lower on decreasing V_G values ($V_{G\ DOWN}$). For the 16 u.c. sample similar results were found.

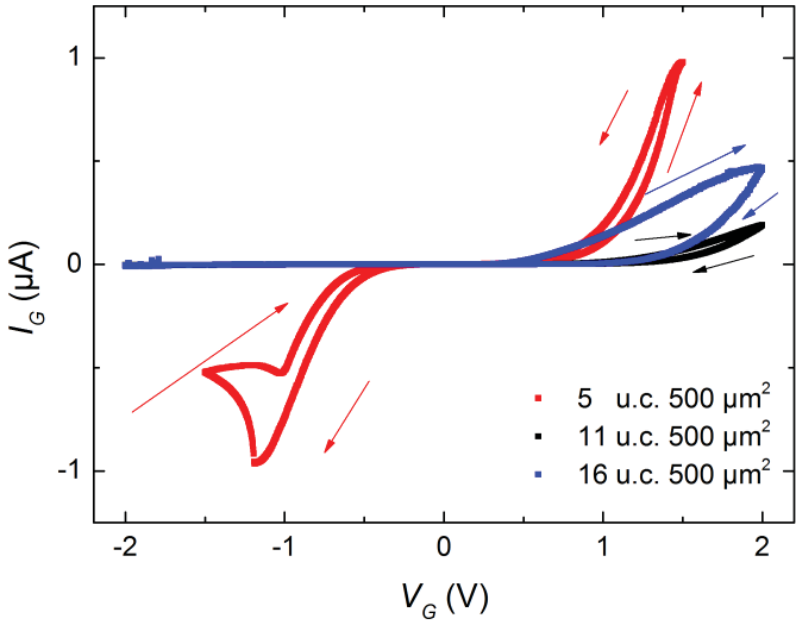

Figure 4.4: I_G as function of V_G for small-area devices on samples with 5, 11 and 16 u.c. LAO as insulator thickness.

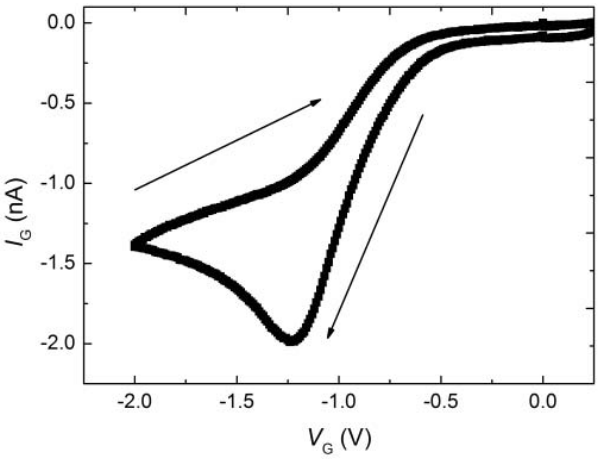

Figure 4.5: $I_G(V_G)$ measured at room temperature on an 11 u.c. LAO device with an area of 117,000 μm^2 averaged over 201 V_G sweeps, showing hysteresis.

4.3.3 Hysteresis as basis for memory

Figure 4.5 shows hysteresis, upon sweeping towards more negative gate voltages, the gate current is higher than when the voltage is swept towards zero voltages. In this figure the maximum I_G ($I_{G\ MAX}$) is at $V_{G\ UP}$ = -1.2 V, the value of I_G ($I_{G\ DOWN}$) at $V_{G\ DOWN}$ = -1.2 V is more than 2 times smaller than $I_{G\ MAX}$. This implicates that one can measure I_G at a read out voltage V_G = -1.2 V and from the value of I_G deduces whether V_G has been higher or lower than -1.2 V before measuring; making the device a kind of memory.

In order to get a larger difference between $I_{G\ MAX}$ and $I_{G\ DOWN}$ a 5 u.c. sample was chosen. For this device with an area of 1000 μm^2 the maximum I_G ($I_{G\ MAX}$) is at $V_{G\ UP}$ = -0.92 V, the value of I_G ($I_{G\ DOWN}$) at $V_{G\ DOWN}$ = -0.92V is more than 10 times smaller than $I_{G\ MAX}$.

To test the stability of the memory, a similar measurement as in Fig. 4.5 was performed, but now as a function of time. Figure 4.6 shows the time dependence of the tunnel current. The top (black) [bottom red] curve has been measured upon increasing the negative gate voltage from 0 to -2 V (in steps of 20 mV every 160 s) [decreasing the negative gate voltage from -2 to -0 V]. The black curve shows a small decrease in gate current in time. Since the decrease of I_G in time is exponential, the difference between $I_{G\ UP}$ and $I_{G\ DOWN}$ is still clear after hours.

The drawback of using the gate current as a memory, is that the maximum is not centered around V_G = 0 V, but at a value between -0.8 and -1.2 V, depending on the device. Therefore, a permanent nonzero gate voltage must be supplied to maintain the state of the memory device. Furthermore, since $I_{G\ UP}$ decreases as a function of time, one cannot discriminate anymore between $I_{G\ UP}$ and $I_{G\ DOWN}$ when the system is at the same potential for a long time.

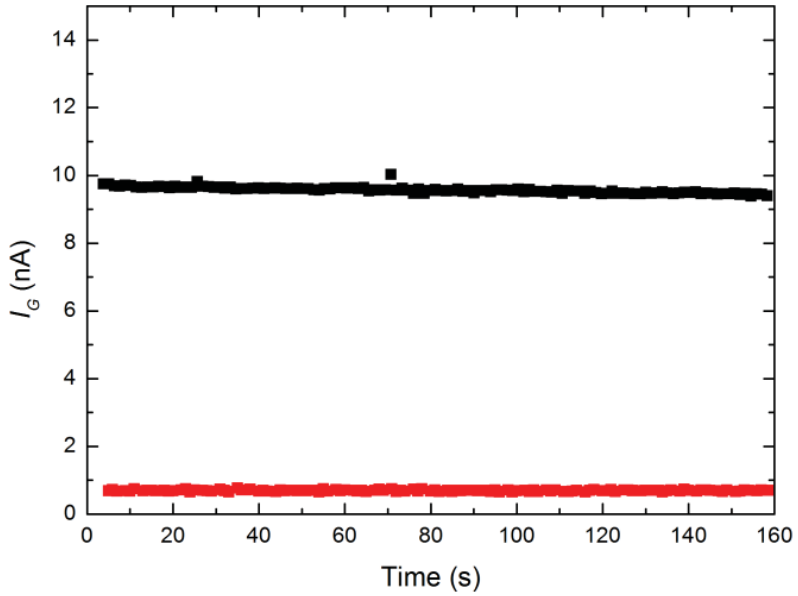

Figure 4.6: Time dependence of the absolute value of the gate current measured at a 5u.c. LAO sample with an area of 1000 µm^2, measured at the maximum of I_G at V_G = -0.92 V. The black (upper) curve has been measured upon increasing V_G towards more negative gate voltages. The red (lower) curve upon decreasing V_G towards 0.

4.3.4 Explanation of the NDR

In section 4.3.1 it was explained why V_G could be decreased to negative gate voltages as large as V_G = -200 V. This was because of the fact that a large enough gate voltage depletes the underlying 2DEG. The NDR has the same origin. Just past the point where I_G has a maximum, the gate voltage starts depleting the 2DEG. Since the amount of charge carriers in the 2DEG decreases, the gate current also decreases. This happens very slowly as a function of time (see Fig. 4.6) but more quickly when increasing the gate voltage to more negative values. The competition between increasing gate current with increasing gate voltage and decreasing gate current due to the depletion of the 2DEG leads to the maximum in tunnel current. Whereas the long relaxation times lead to the observed hysteresis.

4.4 Pressure and temperature dependence of gate current

In order to determine the origin of the tunnel current, i.e. direct tunneling or multi-step via trapped charges in the LAO, I_G (V_G) measurements have been performed at different temperatures. The temperature dependence of I_G could provide information on this issue. To measure this temperature dependence, a 5 u.c. sample was placed in the low temperature probe station. The probe station has been closed and pumped down to a vacuum of around 10^{-4} mbar. After this the system was cooled by a flow of helium that cooled the bottom of the sample via a stage. The temperature was measured at this stage and could be stabilized by a heater, which was linked to a temperature controller.

Figure 4.7(a) shows temperature dependent I_G (V_G) measurements for T = 6, 20, 50, 130 and 170 K. The absolute maximum in I_G around V_G = -1.2 V as was observed for the 11 u.c. device in Fig. 4.5 or for the 5 u.c. device in Fig. 4.3 is clearly shifted towards larger (more negative) V_G with decreasing temperature.

Another remarkable thing is the increase in I_G compared to the 5 u.c. sample measured at room temperature. Compared to Fig. 4.3, I_G increases by more than an order of magnitude for $V_G < 0$ V. Although tunnel current is expected to increase with decreasing temperature, the increase in I_G and the shift of the maximum in I_G observed here is remarkable.

In order to investigate the origin of these changes the gate current of the sample was monitored during the process of pumping down the chamber. In order to have a stable pressure, the pump was connected to the system via a valve and pressure meter. When the pressure meter reached the pressure set point, the valve was manually closed and the measurement was started. After the measurement finished, the valve was opened again until the pressure reached the next set point.

The results of this measurement are displayed in Fig. 4.7(b). What is clear from these measurements is that at room temperature, the pressure influences the gate current. The maximum in I_G at room temperature around 400 nA for this device (red curve) has been shifted to more negative V_G and I_G is higher. Between the ambient pressure gate current (red curve) and the data at 10^{-5} mbar (blue curve) a clear difference exist. The fact that the data at 10^{-2} mbar (green curve) and 10^{-5} mbar (blue curve) hardly differ, indicates that the biggest effect already occurs between 1 bar and 10^{-2} mbar, at relatively high pressure.

Since all low-temperature measurements are conducted in vacuum, it is important to understand what influence the pressure has on the (tunnel) current in the 2DEG system. The LAO/STO system is known to be very surface sensitive. Liquids can, for example change the conductance of the 2DEG[18]. The observed increase in tunnel current as a function of decreasing pressure has not been studied in detail, so only suggestions on the origin of the observed behavior can be made. In line with the report of Xie *et al.*[18] the surface may influence the tunnel current, since water, that is present at ambient pressure, will evaporate from the surface, when the pressure is lowered. The evaporation of water from the LAO/STO leads may affect the tunneling or electric field strength at interface

between the gold top-gate and the LAO/STO leads. Since water is a polar molecule, water molecules bound at the surface will add to the total polar buildup across the LAO. When the water has disappeared from the LAO surface, the total polar moment has decreased, thereby the tunnel barrier may be lowered.

A second explanation may be related to oxygen vacancies in LAO. Those vacancies in an insulator can act as hopping centers for electrons. When the pressure is decreased, oxygen vacancies might be more mobile. If they move towards (or into) the LAO, the tunnel current will increase. Both temperature (Fig. 4.7(a)) and pressure (Fig. 4.7(b)) a relative small effect of the tunnel current on changing show for positive V_G, whereas a negative V_G has a stronger influence. The sign of V_G has been defined as positive when a positive voltage is applied to the top-gate, relative to the 2DEG. A negative V_G thus indicates a negative voltage being applied to the top-gate, making it negatively charged. Atomic oxygen is O^{2-}, so oxygen vacancies are positive charged and attracted by a negative gate voltage. So upon applying a negative gate voltage, oxygen vacancies are attracted towards the top-gate and get trapped in the LAO layer. This gives an intermediate state for tunneling and thereby increases the tunnel current.

At this moment one cannot discriminate between the two suggested mechanisms. Further experiments are needed to be able to do so. For example, heating the sample at ambient pressure to $T > 100\ ^{o}C$, will remove water from the surface, while the oxygen pressure remains unaltered.

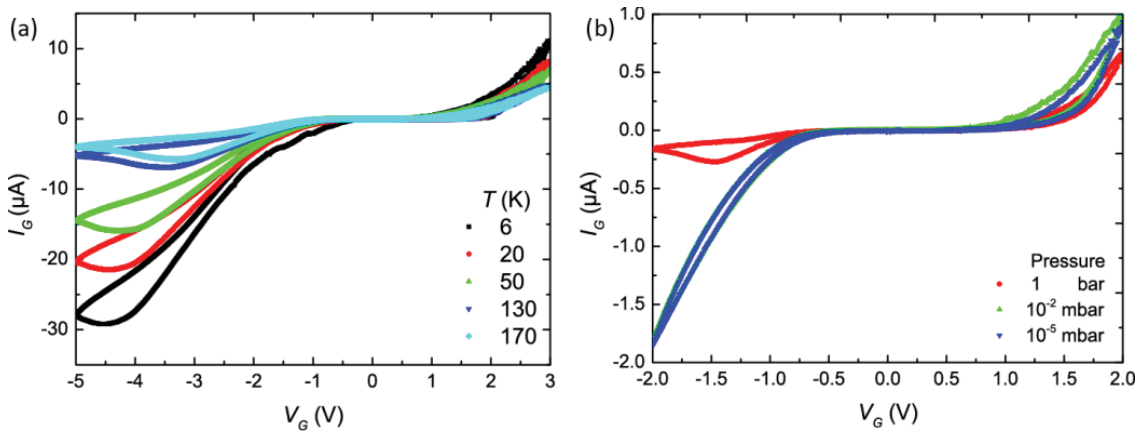

Figure 4.7: (a) Temperature dependence of I_G as function of V_G 5 u.c. (b) Pressure dependence of I_G as a function of V_G measured on a 5 u.c. sample at room temperature.

4.5 Switching the source drain conductivity

Where previous sections focused on the gate current as function of the gate voltage, this and next section will focus on the effects of the gate voltage on the source drain current I_{SD}.

In Fig. 4.3(a) I_{SD} is displayed as a function of V_G for different values of V_{SD}. Figure 4.3(b) shows I_{SD} as function of V_{SD} for different values of V_G. From these figures it is clear that V_G of about -0.8 V is enough to reduce I_{SD} to values below 1 nA. From an application point of view, it would be interesting to know how fast switching between an "on" state (where the 2DEG is conducting) and "off" state(when there is no conduction in the channel between source and drain) would be possible.

From back-gating experiments[14] it is known that the source drain resistance (R_{SD}) changes almost an order of magnitude during a period of 60 s, when the back-gate voltage is switched between 0, -100 and 100 V. The change in resistance at zero applied gate voltage has been attributed to the large voltages that have been applied, changing the oxygen distribution in the film and thereby trapping charges. We may expect a similar behavior between top- and back-gating, although the top-gate voltage used here will be much smaller, the electric field is larger due to the closer proximity of the 2DEG to the gate.

The electric fields generated with top-gating on the 11 u.c. sample described in Fig. 4.3 and Fig. 4.8 are large, they exceed 2.4 x 10^8 V/m (at V_G = 1 V and a distance between top-gate and 2DEG of 4.1 nm). The electric field is this large due to the close proximity of the 2DEG to the gate. For back-gating a typical electric field would be about 4 x 10^5 V/m (at V_G = -200 V and a distance between back-gate and 2DEG of 500 µm). The electric fields differ by almost three orders of magnitude.

The polarization, however, is comparable due to the large dielectric constant of the STO substrate, that is the insulator for back-gating, versus the LAO as insulator for top-gating. For back-gating, assuming ε_{STO} = 20,000 , the polarization is 8 x 10^9 V/m. For top-gating, assuming the bulk LAO dielectric constant ε_{LAO}=25, the polarization is about 5.8 x 10^9 V/m. However, as described in Chapter 5, for thin films the dielectric constant is lower and a value of ε_{LAO} = 7 is more suitable. This leads to a polarization of 1.5 $\times$ 10^9 V/m (at V_G = 1 V). So the polarization that can be achieved with top-gating without gate-leakage is smaller than can be achieved with back-gating, due to the difference in dielectric constants of the gate insulators LAO and STO.

Figure 4.8 shows the response of I_{SD} on switching the top-gate voltage V_G between 0 and -0.8 V as a function of time on a 11 u.c. film, while maintaining a constant source drain voltage V_{SD} =50 mV. For this device V_G = -0.8 V is enough to reduce I_{SD} to < 1nA. This is the "off state". When the gate voltage is set to 0 V, current will flow, the system is in the "on state". When the system is switched from the "on" to the "off" state, the response is

quick, for every switch, there is one data point[ii] slightly above the stable "off" state. However, when the system is switched from "off" to "on" the response is slow. From Fig. 4.8 it can be seen that after 10 seconds in the "on" state, the current still increases. Although I_{SD} still increases after 10 s at V_G = 0 V, the response after 8 times switching is the same as after the first switch. This is different from the first demonstration of switching with a back-gate, where R_{SD} has decreased to half of it original value after only 3 times switching (see ref[14]). So the history of top-gate voltages does not change the conductivity, whereas for a back-gate voltage the history does matter.
(It should be noted that the measurements discussed by Thiel *et al*. [14] have been conducted on a 3 u.c. sample, below the critical thickness of 4 u.c., so the ground state is insulating, in contrast to the conducting 11 u.c. sample discussed in Fig. 4.8).

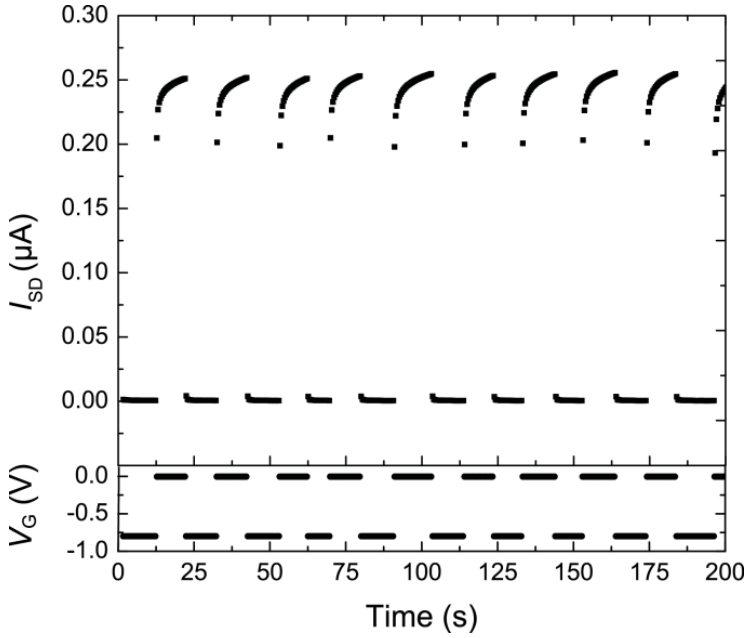

Figure 4.8: Time dependence of the switching of I_{SD} from 250 nA (at V_G =0 V) to < 1 nA (at V_G = -0.8 V) for a fixed V_{SD} = 50 mV

[ii] The measurement has been conducted in such a way that the time between two data points equals one second.

4.6 Carrier density and mobility at room temperature

Different mechanisms exist for determining the carrier density and mobility in 2DEGs. The first mechanism is a Van der Pauw measurement or a Hall-measurement in magnetic field. The advantage is that the power consumption of the device is low. A disadvantage is the need to use a magnetic field. In this section the carrier density and mobility will be determined by a method that is more common to the semiconductor industry. Here, the *I(V)*-curves as a function of gate voltage will be used to determine those values.

Room-temperature measurements have been done on a Hall-bar structure with a LAO thickness of 12 u.c., as displayed in Fig. 3.7(c). Figure 4.9(a) shows *V(I)* curves for applied $V_G \leq 0$ V. Figure 4.9(b) shows *V(I)* curves for applied $V_G \geq 0$ V. The samples have been measured by sourcing current I_{SD} from I_1 to I_2 and measuring the corresponding voltage V_{SD} between V_1 and V_2. A gate voltage V_G has been applied to the top-gate (indicated by V_G) relative to I_2. The measurements have been performed by sweeping I_{SD} from 0 to -2 μA, to 2 μA and back to 0 with a step size of 10 nA. V_G has been stepped from 0 to -2 V, to +2 V and back to 0 with a step size of 0.1 V.

The maxima of V_{SD} for -1.1 V < V_G < 0.9 V for the curves displayed in Fig. 4.9 have been determined and are shown in Fig. 4.9(b) as black dots. For V_G< -1.0 V, no clear maximum can be determined, since the system is close to the insulating state. If there is any conduction left, this is most likely non-uniform. Above V_G > 0.5 V, the maximum V_{SD} seems to decrease. However, this apparent decrease is at the same V_G where gate current starts flowing (see Fig. 4.2). In the intermediate regime both the maximum of V_{SD} and the corresponding I_{SD} show a linear behavior with V_G. The extracted values can be used to calculate the carrier density (n_s) and mobility (μ)[65].

$$n_s = \frac{\varepsilon_0 \varepsilon_{LAO}}{e d_{LAO}} V_{SAT} \qquad (4.1)$$

Where ε_{LAO} is the dielectric constant of LAO. d_{LAO} is the thickness of the LAO insulator layer. V_{SAT} is the maximum value of the *V(I)* curve, *e* is the electric charge and ε_0 the permittivity of vacuum.

$$\mu = 2 \frac{I_{SAT} d_{LAO}}{\varepsilon_0 \varepsilon_{LAO} V_{SAT}^2} \frac{L}{W} \qquad (4.2)$$

Where I_{SAT} is the I_{SD} at V_{SAT} , *L* is the length of the conducting channel between the voltage probes and *W* is the width of the channel.

Using these formulas the carrier density (n_s) and mobility (μ) have been calculated for several V_G. It should be noted that ε_{LAO} plays a role in both the carrier density and mobility and is unknown. Figure 4.10. has been made with the assumption that ε_{LAO} equals the bulk value of 25 at room temperature. In this figure the carrier density is

displayed in black and has been fitted with a linear fit between -1.0 V ≤ V_G ≤ 0.5 V, this fit is displayed in red. The data clearly shows linear behavior, save for the points where I_G increases or where the n_s gets small.

At V_G = 0 V, n_s = 20 x 10^{13} cm^{-2}, when we compare this value to room-temperature measurements using a Hall-bar in a magnetic field, these values are within the same order of magnitude, see for example Fig. 3.2. The calculated mobility of 1-2.5 cm^2/Vs is also close to the values extracted from Hall measurements. From these results we can conclude that there is no significant difference between the two methods.

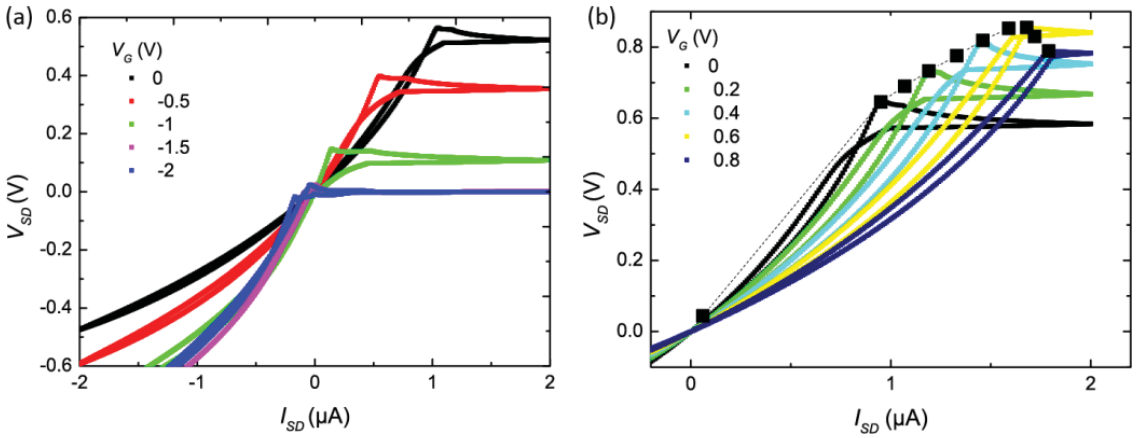

Figure 4.9: *V*(*I*) curves as function of (**a**) negative or (**b**) positive V_G for a 12 u.c. LAO Hall-bar at room temperature. The black dots indicate $V_{SAT}(I_{SAT})$.

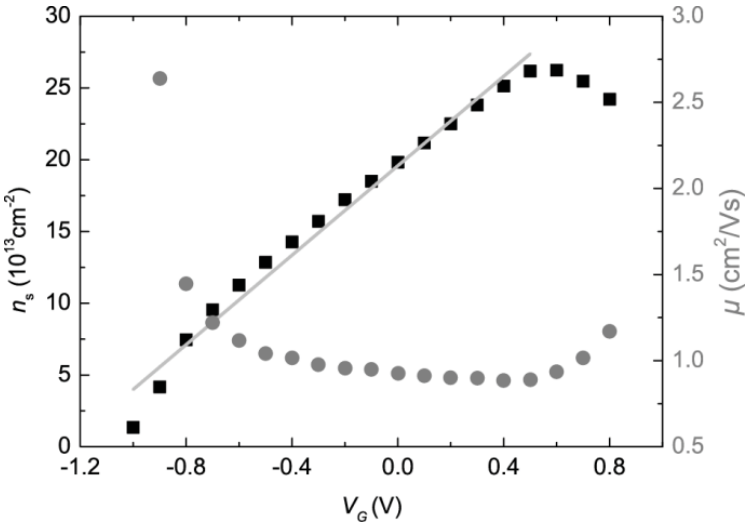

Figure 4.10: Mobility (gray circles, right axis) and carrier density (black squares, left axis) at room temperature as a function of gate voltage calculated from the $V_{SD}(I_{SD})$ measurements shown in Fig. 4.9. The line is a linear fit to the carrier density as function of gate voltage.

4.7 Conclusion

In this chapter it has been demonstrated that by applying an electric field, the conductivity of the 2DEG between LAO and STO can be influenced. A negative gate voltage can deplete the underlying 2DEG, whereas a positive gate voltage increases the carrier density. The most important discovery is that this gating can be done, within certain boundaries, without suffering from the gate current: the gate current from top-gate to 2DEG is the lowest reported in literature. Depending on the thickness of the LAO layer, the magnitude of the gate current changes. For the samples with an LAO thickness of 11 and 16 u.c. the gate current is small when a negative gate voltage is applied. For the thinner, 5 u.c. sample, the gate current is larger. It has been shown that this gate current as a function of gate voltage shows hysteresis. It is argued that this hysteresis is a result of the depletion of the 2DEG and the slow recovery to the conducting state. Also a negative differential resistance in the tunnel current is observed. This results from a competition between tunneling and depletion of the 2DEG.

Further research could be done on the full understanding of the tunnel mechanism. However, one should take into account that by applying a gate voltage, the depth of the 2DEG is influenced: the effective electric field may be non-linear with the applied gate voltage.

The fact that the gate current increases when the sample is in vacuum could be studied in more detail. This is important, since all low temperature measurements are conducted in vacuum. If one can avoid this increase in gate current at low pressures, larger electric fields can be applied at low temperatures.

Chapter 5

Tuning (super)conductivity by top-gating

This chapter covers low temperature measurements on top-gated LAO/STO samples. It covers gate current at low temperature, measurements on the carrier density to determine the dielectric constant, tuneable superconductivity, the insulating state that appears at negative gate voltages and some peculiar oscillations from magnetotransport data.

5.1 Introduction

The previous chapter showed room-temperature data of top-gated LAO/STO interfaces, among this were depletion and enhancement of the 2DEG and the gate current dependences on gate voltage, pressure and temperature. From a general point of view measurements at low temperature are interesting, since there is less disturbance from lattice vibrations. For the specific case of LAO/STO the carrier density and mobility are strongly temperature dependent. Upon decreasing temperature, the carrier density of the LAO/STO interface decreases, due to the freeze out of thermally activated charge carriers. At the same time the mobility increases. Interesting physics appears at the lowest temperatures, as quantum effects start to influence the resistance. Around T = 2 K the system shows for example weak (anti-) localization or Shubnikov-de Haas oscillations. These quantum phenomena become clearer at lower temperatures. Further lowering of the temperature may lead to superconductivity. It has been demonstrated that many of the quantum effects can be tuned by means of back-gating. In this chapter the focus will be on low-temperature top-gating effects on quantum effects and (super)conductivity. The work discussed in this chapter has been conducted on two top-gated Hall-bar devices, as displayed previously in Fig. 3.7 (c). The distance between two voltage probes is 200 µm, whereas the width of the Hall-bar is 20 µm (Hall-bar 1) or 15 µm (Hall-bar 2). The thickness of the LAO layer is 12 u.c., approximately 4.5 nm.

5.2 Gate current at low temperatures

In Chapter 4 the effects on the conductivity of the LAO/STO interface upon applying gate voltage at room temperature have been discussed. The temperature dependence of the gate current (as shown in Fig. 4.7(a)) showed an increase in gate leakage with decreasing temperature for negative gate voltages, at the same time the gate current at positive gate voltages decreased. Since in this chapter the focus will be on the influence of the gate-voltage on the electrical transport properties of the 2DEG, the gate current should be negligibly small. To test if this is the case, the gate current (I_G) has been measured at a temperature of T = 37 mK as a function of gate voltage (V_G), this is displayed in Fig. 5.1. The figure shows that I_G < 1 nA for -0.5 V < V_G < 1.5 V. This gate current is 3 orders of magnitude smaller compared to the usual source drain current (I_{SD}) of 1 µA. The inset (on logarithmic scale) demonstrates that when the gate current exceeds 1 nA, the gate current rapidly increases when the gate voltage is increased further. This significant, unwanted gate current can cause problems due to heating, or due to the fact that the current flow is no longer solely in the 2DEG and therefore not well defined anymore. These problems (at high gate voltages) will be addressed later in this chapter.

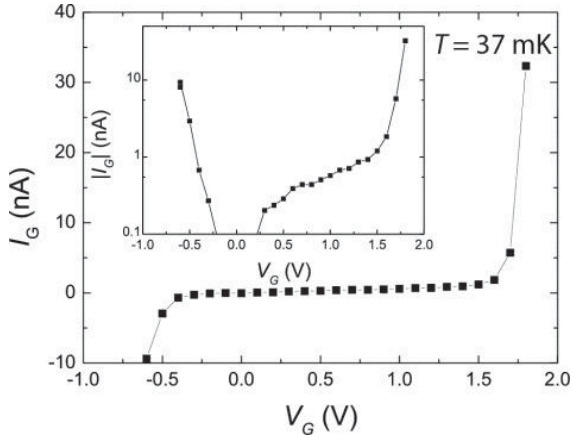

Figure 5.1: Gate current as a function of gate voltage at *T*= 37 mK

5.3 Dielectric constant of a thin layer $LaAlO_3$

Transport measurements have been performed in a Quantum Design Physical Properties Measurement System (PPMS). The internal hardware of the system has been used to source I_{SD} and measure V_{SD}. An external voltage source (Keithley 2400) has been used for applying V_G. V_G is applied to the top-gate, relative to the ground, connected to V_D. The PPMS measurements have been performed on a Hall-bar that has been defined using the methods described in Chapter 3. The sample had a thickness of 12 unit cells and the aspect ratio between width and length was 10. Figure 5.2 shows the Hall resistance as function of magnetic field, for different V_G. The curves are linear, indicating one-band conductance. After subtracting a linear background, the residual resistance is less than 2 Ohms, for all studied magnetic fields and all V_G except for V_G = -0.3 V, where quantum oscillations are visible after subtracting a linear fit, this will be discussed in more detail in section 5.6. The low value of the residual resistance indicates that a linear fit is appropriate and the one band assumption is valid. From these linear fits the carrier density (n_s) can be obtained as a function of V_G. This is displayed in Fig. 5.3. The observed n_s at V_G= 0 V is 1.9×10^{13} cm^{-2}, very close to the nominal carrier density of $2 \times 10^{13} cm^{-2}$ for LAO/STO interfaces without top-gate. This observation is of importance, since previous attempts to fabricate a top-gate[15] (using YBaCuO as a top-gate) resulted in a carrier density that was only 10% of the nominal value. In our experiments we observe that with increasing V_G the carrier density increases, whereas a negative V_G results in a lower carrier density. This is in line with back-gating measurements[66], where the same trend in the gate dependence of the carrier density has been observed. Although the electrical field is oriented differently (pointing down for positive top-gating and up for back-gating), the resulting electrostatic force is still positive, attracting electrons towards the interface. A negative V_G pushes electrons away from the interface, deeper in the STO (top-gating) or into the LAO towards the surface (back-gating). As expected, the voltage needed for changing the carrier density using a top-gate is more than two orders of magnitude

smaller than in the case of back-gating, where the effective distance between 2DEG and gate is much larger.
The system can be considered to be a simple parallel plate capacitor, with the top-gate as one of the conducting plates, the 12 u.c. LAO as the insulator and the 2DEG as the second plate. The capacitance of the device can be calculated by

$$C = \frac{A*\varepsilon_0*\varepsilon_{LAO}}{d_{LAO}} , \quad (5.1)$$

where *C* is the capacitance, *A* is the total area of the capacitor, ε_0 and ε_{LAO} are the dielectric constant of vacuum and LAO, respectively, and d_{LAO} is the thickness of the insulating (LAO) barrier. When the total amount of charge is known, the linear fit in Fig. 5.3 can be used to calculate the dielectric constant of the LAO. The total charge *Q* is given by

$$Q = n_s * e * A, \quad (5.2)$$

where n_s is the carrier density and *e* is the charge of an electron. Since

$$C = \frac{\Delta Q}{\Delta V}, \quad (5.3)$$

Eq. 5.2 can be inserted in Eq 5.1 and this can be solved for ε_{LAO}. From these formula a dielectric constant of ε_{LAO}= 7 is extracted for the LAO insulator. This is lower than the reported values for thick LAO at room temperature (ε_{LAO}= 24). Recently very similar values (ε_{LAO}= 6-8) for thin films of LAO at low temperatures have been reported[67]. In this report the LAO capacitor was modeled as a “dead” layer in series with an ideal bulk LAO insulator. This “dead” layer occurs at the interface between the LAO and gold, due to in diffusion of gold or roughening of the LAO and has a lower dielectric constant. Using

$$\frac{d_{LAO}}{\varepsilon_{LAO}} = \frac{d_{LAO}-d_{dead}}{\varepsilon_{bulk}} + \frac{d_{dead}}{\varepsilon_{dead}}, \quad (5.4)$$

where ε_{dead} and ε_{bulk} are the dielectric constant of the “dead” layer and the bulk dielectric constant of LAO, and d_{dead} is the thickness of the “dead” layer. Since we have not measured a thickness dependence of the capacitance, there are too many unknowns in Eq. 5.4 to solve. When we take the values for ε_{dead} = 4.3 and d_{dead}= 4.3 u.c. from Ref. [[67]], a bulk value of ε_{bulk}= 11 is obtained. This does not differ much from the measured dielectric constant of 7 and is still off from the actual bulk value. A d_{dead}= 6.4 u.c. is needed to obtain the bulk value of 24 for ε_{bulk} when ε_{dead}= 4.3 is used. When we reconsider what

the dead layer is, it is the interface between gold and LAO, which is behaving as a bad insulator. An estimated ”dead” thickness of 4.3 or 6.4 u.c. is big for an interface effect. Furthermore, the estimated ε_{dead} of 4.3 is high for a bad dielectric and the fit in Ref.[67] is far from perfect. Assuming ε_{dead}= 1, a thickness of the dead layer of 1.2 u.c. is obtained, a value that may be closer to the physical reality (if the “dead” layer originates in diffusion of gold or roughening of the LAO). The big spread in possible solutions for the thickness and dielectric constant of the “dead” region near the LAO/gold interface in Eq. 5.4 to obtain ε_{bulk}= 24, can be explained by the fact that $\frac{d_{LAO}-d_{dead}}{\varepsilon_{bulk}} \ll \frac{d_{dead}}{\varepsilon_{dead}}$. The latter ratio dominates the solution, therefore a thickness dependent measurement of the dielectric constant is needed to find the thickness and dielectric constant of the “dead” layer in our samples. To conclude: a thin dead layer at the interface between the top-gate and the insulator can significantly lower the measured dielectric constant, since the dielectric is very thin. And the measured dielectric constant of 7 is in agreement with existing literature.

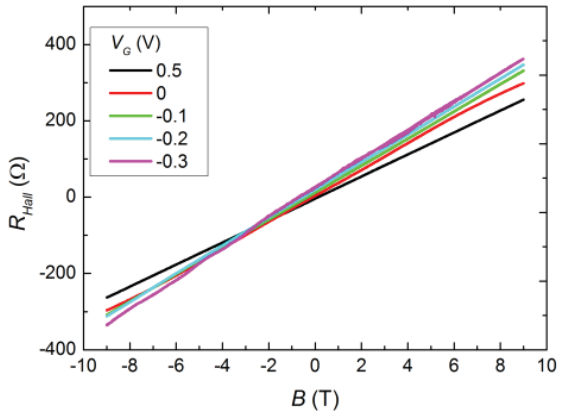

Figure 5.2: Hall resistance as a function of magnetic field for different gate voltages, measured at *T* = 2K.

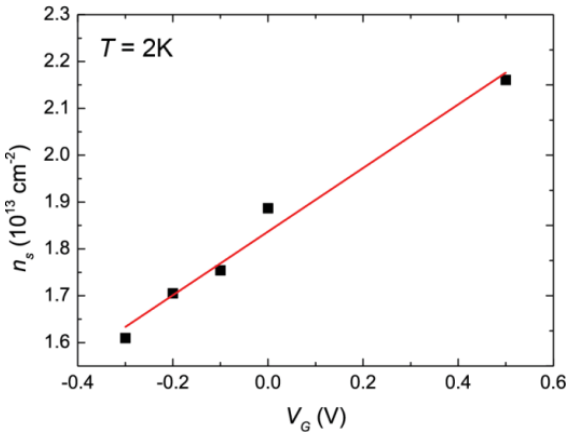

Figure 5.3: Carrier density as function of gate voltage, extracted from the Hall resistance curves in Fig. 5.2. Error bars are within the symbol size.

5.4 Tunable superconductivity in top-gated LAO/STO

When the LAO/STO interface is cooled down to about 250 mK, the system becomes superconducting. Figure 5.4(a) shows typical $I(V)$-curves for Hall-bar measurements (on Hall-bar 2) of the longitudinal voltage at temperatures between 35 mK and 275 mK, at V_G= 0 V. At T= 275 mK the system is in a resistive state, upon lowering the temperature, the superconducting state (V = 0 V) appears. The critical current I_C, which is defined as the highest current that can be passed through the system without dissipation (V_{SD} = 0 V), increases with decreasing temperature, as expected. When a gate voltage V_G is applied to the system the temperature-dependent resistance R changes as indicated in Fig. 5.5. Figure 5.5(**a**) shows the measured gate voltage dependence of R for different temperatures for a fixed I_{SD} = 110 nA. Temperatures below 200 mK are not displayed; they overlap with the 200 mK data, since for all applied V_G the system is in the superconducting state below this temperature. The figure shows that increasing V_G increases the critical temperature. Figure 5.5(**b**) shows the same data, plotted as function of temperature. A possible suggestion for the disappearance of superconductivity above V_G = 1.3 V is that when V_G > 1.3 V, a large gate current (I_G > 10 nA) flows. Due to this current flow, energy is dissipated and heat is generated, leading to a local increase in temperature. This temperature due to heating is in the order of (or exceeds) the critical temperature of the interface. Therefore the curves measured above V_G = 1.3 V show a sudden reappearance of resistance.

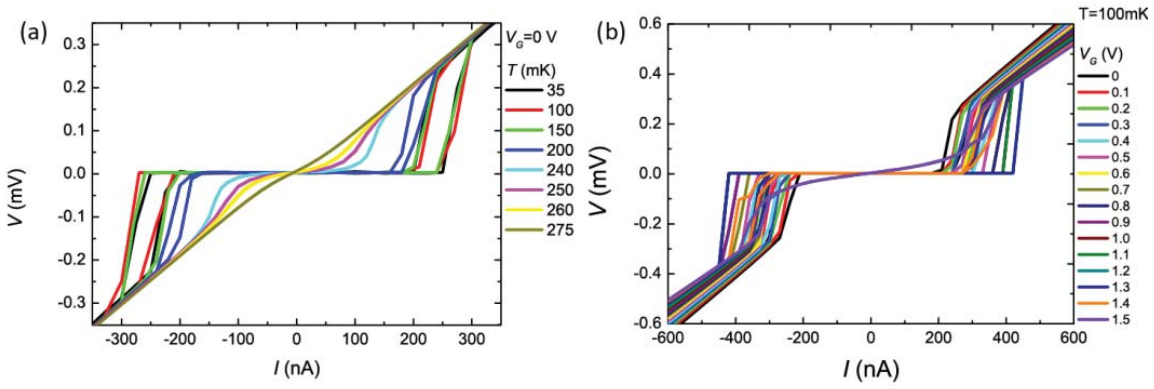

Figure 5.4: (**a**) $I(V)$-curves as function of temperature with V_G = 0 V. (**b**) $I(V)$-curves as function of gate voltage at T = 100 mk

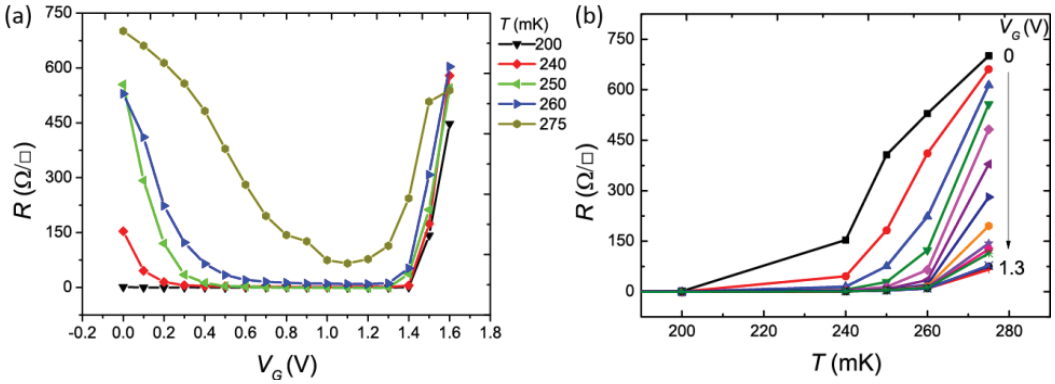

Figure 5.5: (**a**) Gate voltage dependence of the resistance (at I_{SD}= 110 nA) for temperatures close to the critical temperature (**b**) Temperature dependence of the resistance for different gate voltages at a fixed I_{SD} = 110 nA. Lines are guides to the eye.

The gate voltage dependence of the *I*(*V*)-measurements at a fixed temperature (*T* = 100 mK) is displayed in Fig. 5.4(b). From this figure, the increase in critical current with increasing V_G is obvious. The gate current (or the associated heat) leads to a lower I_C at V_G = 1.4 V and does not allow the system to reach the superconducting state at V_G = 1.5 V. These measurements all showed only the positive gate-voltage dependence of Hall-bar 2. Figure 5.6 shows both positive and negative gate-voltage dependence of *I*(*V*)-measurements on Hall-bar 1 at *T* = 37 mK. Figure 5.6(a) shows *I*(*V*)-curves for V_G between -0.6 V and 2 V in steps of 0.2 V. Figure 5.6(b) is a color plot of Fig. 5.6(a) , where the superconducting area between -0.6 V and 1.5 V is displayed in green. The positive gate voltages show a similar trend as described before, it increases the critical current. A negative gate voltage reduces the superconductivity and can even turn off the superconductivity when the gate voltage is as low as -0.6 V, see the most left *I*(*V*)-curve in Fig. 5.6(a).

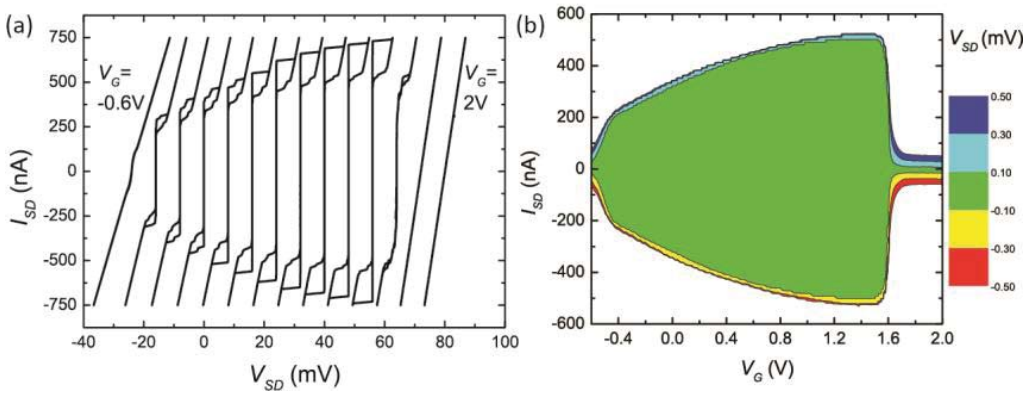

Figure 5.6: (**a**) *I*(*V*)-curves for different gate voltages, V_G. Curves are shown in steps of 0.2 V and offset for clarity. (**b**) Color plot of the data shown in (**a**), the green color indicates the superconducting region. Measurements performed at *T* = 37mK

5.5 Insulating state

In Fig. 5.6 the most negative gate voltage applied is V_G = -0.6 V. At this voltage a very small critical current can still be observed, but the system is close to the insulating state. The LAO/STO undergoes a transition from (super)conducting to insulating upon applying a large negative electric field. It turned out to be impossible to go to more negative electric fields and measure a reproducible $I(V)$-curve. The observation of a transition from superconducting to insulating has been reported before for back-gated structures[35]. In the case of back-gating this phase transition is fully reversible. In the top-gated devices reported here, conductivity could not be recovered once the system entered the insulating state, unless the temperature was raised above a certain limit. This has been tested by slowly heating the dilution refrigerator from base temperature to room temperature and meanwhile measuring $I(V)$-curves. Only after raising the temperature above T = 160 ± 2 K, the $I(V)$-curves became linear again. A cool down after exceeding this recovery temperature resulted in superconducting $I(V)$-curves, as in the initial cool down. It is noted that in recent studies[68, 69] the same temperature was needed to restore initial cool down conductivity.

Applying a positive gate voltage and decreasing it afterwards, does not irreversibly change the 2DEG, although the gate current has reached the maximum gate current (threshold value) of 300 nA at high V_G. A small hysteresis between increasing V_G and decreasing V_G of about ΔV_G= 0.1 V is observed. For negative gate voltages, the cross over to the insulating state does not always occur at the same V_G. We observe that the individual voltage contacts started to become disconnected from the Hall-bar at V_G = -0.2 V. The Hall-bar itself reaches the insulating state at an applied V_G between -0.4 V and -0.7 V. The insulating state can be described by a non-linear, non-reversible $I(V)$-curve. A two-point measurement shows a resistance larger than 1 GΩ. However, a four-point measurement at a constant current bias, still measures a finite voltage difference between the voltage contacts. This voltage should not be used to calculate a resistance, because it is not linear with the current. So when four-point measurements are done at a constant current bias, one has to be sure that the $I(V)$-curves are linear, for example by measuring an $I(V)$-curve before and after measurements.

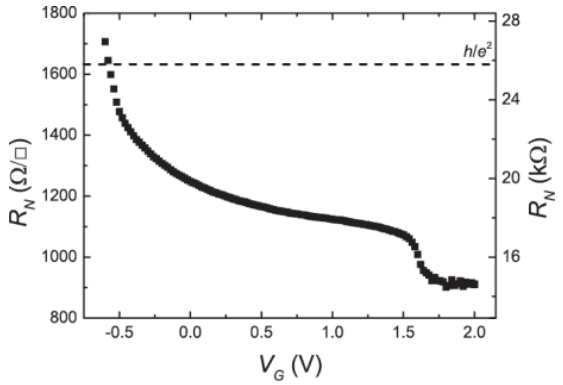

Figure 5.7: Normal state sheet resistance as a function of V_G (left axis) and normal state resistance of the whole Hall-bar (right axis), showing a large increase in resistance to a value close to h/e^2 = 25.8 kΩ (right axis) near the metal/insulator transition at V_G = - 0.5 V, measured at T = 37 mK, above the critical current.

In order to find the origin of the insulating state, the normal state resistance has been plotted against gate voltage in Fig. 5.7. The normal state resistance in this figure has been extracted from the linear part of the $I(V)$-curves in Fig. 5.6, above I_C. The sheet resistance values (left axis) in this figure are not close to the quantum resistance $h/2e^2$, but only about 10-15% of this value. One expects an insulating state for a sheet resistance larger than the quantum resistance and a metallic behavior when the sheet resistance is smaller[70]. The insulating state clearly appears already when the sheet resistance is below the quantum resistance. However, the resistance of the total area under the gold top-gate (right axis) does exceed the quantum resistance. The total resistance below the top-gate can be calculated: based on the Hall-bar dimensions this is 16 times the value of the sheet resistance. The total resistance between the current source and drain is plotted in Fig. 5.7 (right axis). In this figure also a line indicating h/e^2 is indicated. Close to this value (around V_G= -0.5 V) a sharp increase in resistance as function of V_G is noted. The resistance h/e^2 is a factor of 2 higher than expected for the metal-insulator transition[70]. More study is needed to explain this difference.

It should be noted that in the work of Hosoda *et al.*[67] a value of about 13 kΩ ~ $h/2e^2$ can be calculated for the total resistance between the voltage probes. To calculate this value, it has been assumed that they also observe a metal-insulator transition. Since the mobility is higher in their case, they are able to gate the 2DEG to lower carrier densities, but keeping the total resistance below the quantum resistance. Under the assumption that the lowest mentioned carrier density is the lowest they could measure, and taking in account the corresponding mobility and the aspect ratio (30), this value of resistance could be calculated. From their paper it is not clear how much their top-gate extends outside the voltage-probes of the Hall-bar, which is needed in order to calculate the total resistance between the current contacts. However, the values are the same order of magnitude and between $h/2e^2$ and h/e^2, whereas the sheet resistance at the cross-over between metal and insulating differs by a factor of 3. Remarkably not the sheet resistance,

but the total resistance below the top-gate is close to the quantum resistance. The origin of these observations and the driving force for the metal-insulator transition are still open questions.

5.6 Quantum oscillations

Shubnikov-de Haas oscillations can be observed at sufficiently low temperature in a 2DEG. The 2DEG should have a sufficiently high elastic scattering time, in other words a sufficiently high mobility, since the requirements for observing these quantum oscillations are:

$$\omega_c < \tau, \tag{5.6}$$

And

$$\hbar\omega_c > k_B T, \tag{5.7}$$

where $\omega_c = \frac{eB}{m_e}$ is the cyclotron frequency, τ is the elastic scattering time, k_B is the Boltzmann constant, *T* is the temperature, m_e is the effective carrier mass and *B* is the perpendicular magnetic field.

In the longitudinal resistance the Shubnikov-de Haas effect appears as oscillations. These oscillations are periodic in 1/*B*, when one electronic band is contributing to the conductivity. A one-band model has been used to fit oscillations in the work of Caviglia *et al.*[19] and Ben Shalom *et al.* [20]. It is known that multiple bands play a role in the conductivity at the LAO/STO interface[44]. In Fig. 2.4 a schematic band picture of the LAO/STO 2DEG near the gamma point was shown. Depending on the location of the Fermi level, one or more bands contribute to the conductivity. When more than one band contributes to the conductivity, a multi-band model needs to be used. In the work of McCollam *et al*.[21] up to 5 different bands were needed to be able to fit the oscillations. It should be noted that the material system used by McCollam *et al*. consisted of LAO/STO with a $SrCuO_3$/STO capping, which significantly lowers the carrier density, thereby changing the main conducting band from the d_{xz} to the d_{xy} band. The change of the bands may have altered the transport properties, since the d_{xy} band contains carriers with a lower effective mass.

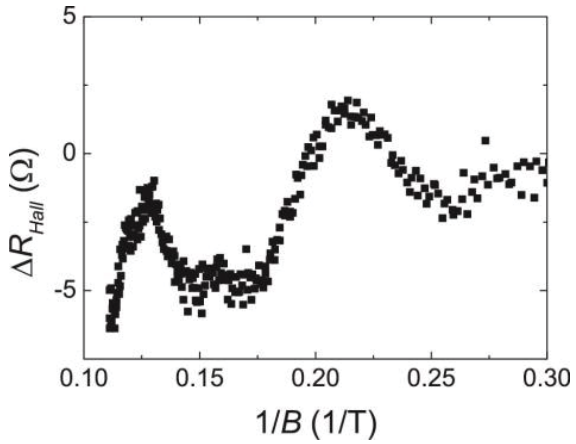

Figure 5.8: Oscillations in the Hall resistance at V_G= -0.3 V after subtracting a linear fit to the data in Fig. 5.2.

It has been demonstrated that the Shubnikov-de Haas oscillations in a 1-band model can be tuned by applying a back-gate voltage.[19, 20] Since an electric field can change the carrier density, mobility and effective mass in the LAO/STO system, quantum oscillations appear and can be tuned by the electric field.

Using top-gating the carrier density can be tuned, as is clear from Fig. 5.3. The change in mobility will be discussed in the next chapter, but is quite small (few %), based on transport measurements. The surprising thing is that although the mobility is low in the sample discussed here (about 200 cm^2/Vs), oscillations in the resistance appear when a negative gate voltage is applied. When a linear fit is subtracted from the data in Fig. 5.2., the residual resistance is less than 2Ω for all values of B, for all applied V_G, except for the most negative value of V_G, V_G=- 0.3 V. The residual resistance for this particular gate voltage shows oscillations. These are plotted as function of 1/B in Fig. 5.8. If these oscillations were a result of a longitudinal component in the Hall-resistance, the oscillations should be observed in the longitudinal resistance at this gate voltage. However, at this gate voltage, the longitudinal resistance does not show quantum oscillations. During several other cool downs, oscillations in the Hall-resistance have been observed without measuring them in the longitudinal resistance. At the same time oscillations in the longitudinal resistance do not always coincide with oscillations in the Hall-resistance. So it is doubtful whether or not a longitudinal component of the resistance is the reason for the observation of quantum oscillations in the Hall-resistance.

In a very clean 2D system, with high mobility, the quantum Hall effect (QHE) can be observed. In oxides this has been observed in the ZnO/MgZnO system[71]. In the same system at a mobility exceeding 500,000 cm^2/Vs, the fractional QHE has been observed[72]. From back-gating experiments it is known that training of the system is needed to get reproducible measurements. This training can be done by applying a large electric field for at least half a day. The effect discussed below may also originate from a training effect, since the experiment has been conducted at V_G = 0 V, after 6 hour long measurements at

V_G = 1.5 V, 1 V and 0.5 V. The system has been at a positive gate voltage for a total time of 18 hours. Figure 5.9 shows the Hall resistance (R_{xy}) and longitudinal resistance (R_{xx}) as function of magnetic field at zero gate voltage at a temperature of 37 mK. In R_{XX} plateaus can be observed in the resistance as a function of magnetic field. The thick black lines indicate the end of a plateau and have been extended to the top of the figure, where R_{xy} is displayed. The Hall resistance is very non-linear, noisy and has a large offset. But local maxima and minima can be observed. And it appears that the end of the plateaus in R_{xx} coincide with a local maximum or minimum in R_{XY}, as indicated by the thick black lines. Furthermore at approximately the same positive and negative magnetic fields values, the plateaus end. However, these plateaus appear in the longitudinal resistance, instead of in the Hall resistance in case of the QHE. The observation of maxima in conductivity is expected to appear in the longitudinal resistance and not in the Hall resistance as observed here. So if this effect is related to the QHE, the mechanism must be unconventional. More study and a theoretical understanding are needed to explain this observation.

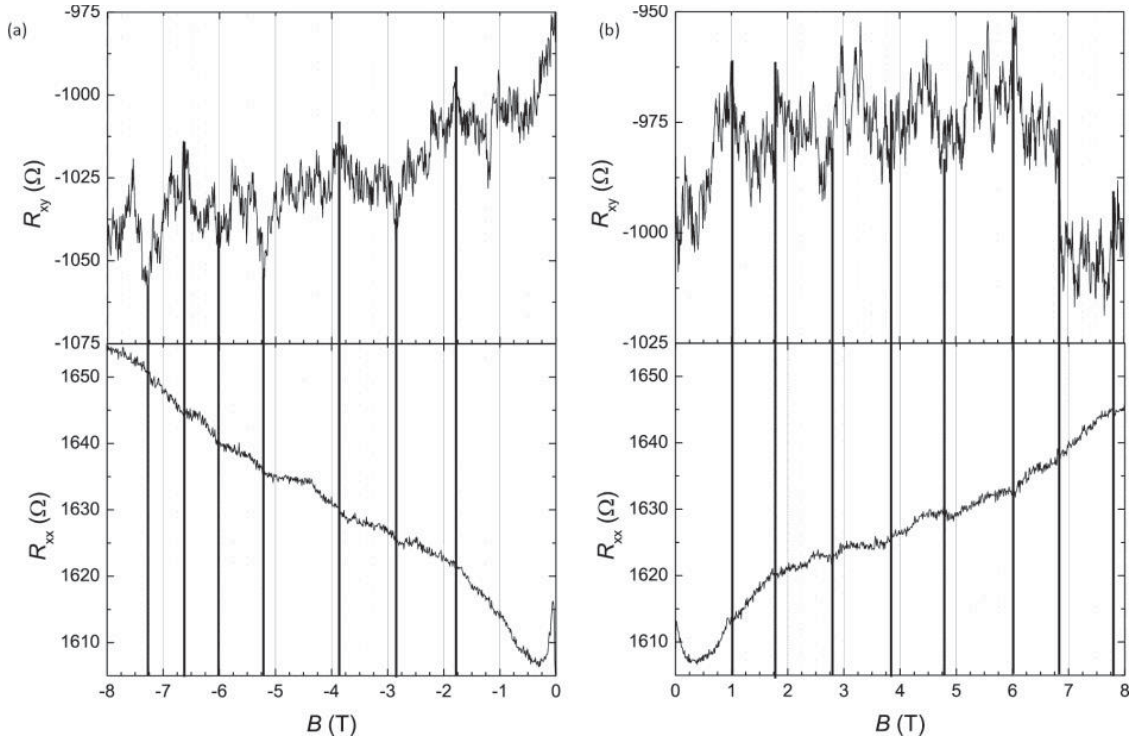

Figure 5.9: Steps in the longitudinal resistance (R_{xx}) in negative (**a**) and positive (**b**) magnetic field at magnetic field values where a local maximum or minimum in the Hall-resistance (R_{xy}) appears.

5.7 Conclusion

In this chapter the low temperature measurement results of top-gating studies on the LAO/STO 2DEG were presented. It was demonstrated that the carrier density can be tuned by applying a top-gate voltage. A negative top-gate voltage decreases the carrier density, whereas a positive top-gate voltage enhances it. This is in agreement with back-gating experiments. It has been shown that the carrier density at zero gate voltage is comparable with samples without back-gate, so the gold electrode on top of the LAO does not influence the carrier density.

The superconductivity in the sample can be modulated by the application of an electric field via the top-gate. An increase in critical temperature and critical current density of the 2DEG can be observed when a positive gate voltage is applied. In back-gating studies hundreds of Volts need to be applied to see an effect on the superconducting critical temperature. Whereas in this work only voltages below 2 V were used to observe an increase in the critical current and critical temperature. It is the first time that it has been demonstrated in the LAO/STO material system that the superconductivity can be modified by applying an electric field from a top-gate.

A “problem” during the measurements was the fact that the sample reached an insulating state when a negative gate voltage was applied. This seems to be related to the resistance of the Hall-bar. However more research is needed to explain this insulating state. Further research should also explain why the system needs to be heated up to a temperature of 160 K before it becomes conducting again. A last suggestion would be to use a LED or laser to introduce photo carriers at low temperatures and use these to refill the depleted 2DEG.

The last part of the chapter describes the observed oscillations in the Hall resistance and the plateaus in the longitudinal resistance. This is surprising, since if these would originate from the Quantum Hall Effect, the effects should occur in the other measurement channel. More research is definitely needed to make a real statement about this observation.

Chapter 6

Spin-orbit coupling in top-gated $LaAlO_3$-$SrTiO_3$

This chapter covers the analysis of magnetotransport data that showed weak-anti-localization. By fitting the data according to the Maekawa-Fukuyama theory we could extract values for spin-orbit relaxation time. We demonstrate stronger spin-orbit coupling when a positive electric field is applied by top-gating. Since the mobility does not change as function of gate voltage, we could not determine the spin-orbit relaxation mechanism.

6.1 Introduction

After the discovery[5] of a 2-dimensional electron gas (2DEG) between insulating $LaAlO_3$ and $SrTiO_3$, many interesting phenomena have been observed at the conducting interface. Magnetism[22, 29], superconductivity[33] and surprisingly the co-existence[31, 37] of both, normally counteracting each other. Bert *et al*.[31] observed superconductivity and ferromagnetism in patches using a scanning SQUID microscope. Li *et al*.[37] also measured magnetism and superconductivity on a single sample. They found a strong magnetic signal in torque magnetometry and low-temperature transport measurements showed superconductivity.

One of the other phenomena which has been observed, is Rashba spin-orbit coupling. Caviliga *et al.*[24] showed tunable spin-orbit coupling. They applied a voltage to a back-gate to change the peak in the conductance that appeared due to weak anti-localization at zero magnetic field. Using the Maekawa-Fukuyama (MF) theory[73] they were able to identify the spin-orbit relaxation mechanism to be of Dyakonov-Perel[74] (DP) type. Other groups also reported on tunable spin-orbit coupling using back-gating to tune the magnetoresistance (MR) in a parallel field[38] or perpendicular field[23, 75].

To explain the co-existence of superconductivity and magnetism, it has been suggested that different bands in the LAO/STO contribute to different phenomena. It is generally assumed that the conductivity at the interface occurs from the Ti 3d electrons. Those 3d electrons can occupy different t_{2g} orbital states. The degeneracy of those orbital states is lifted at the interface. Several models[39, 40, 76] assume the d_{xy}-electrons to be confined to the interface. Coulomb interaction between the mobile d_{xz} (or d_{yz}) electrons and the localized d_{xy} electrons in combination with the spin-orbit coupling in the d_{xz} (or d_{yz}) band, enable a model where spin-orbit coupling can couple patches of superconductivity through a magnetic background[40]. The superconductivity must thus be carried by the d_{xz} (or d_{yz}) electrons. The model is supported by the fact that samples exist that do not have mobile electrons in the d_{xz} (or d_{yz}) band, such as STO/LAO/$SrCuO_3$/STO samples[16]. Those samples have a lower carrier density and the conductivity in this system is suggested to take place through the d_{xy} electrons[77]. As expected from the model, those samples do not show superconductivity[16].

6.2 Quantum corrections to resistivity

When a current is sent through a material a voltage drop occurs, since electrons moving in the material will suffer certain scatter events, where energy is lost. Scatter mechanisms are for example interactions between electrons and phonons or other electrons. They can be divided in two groups: elastic scattering and inelastic scattering. The inelastic scattering time τ_i is the average time between two inelastic scatter events, where energy and phase

information are lost. The elastic scattering time τ is the average time between two elastic scatter events, where the momentum (direction) of the electron is changed, but the energy and phase remain the same.

Scattering of electrons is a random process, therefore it is possible that electrons arrive at their original location after certain elastic scatter events. There is phase coherence between the point of departure and arrival when the elastic scattering time is larger than the inelastic scattering time, $\tau > \tau_i$, and the length of the trajectory is shorter than the corresponding inelastic scattering length. Figure 6.1 shows a schematic of a few elastic scatter centres and lines that indicate the trajectories electrons can travel. As shown in the figure, electrons can travel the same path in opposite directions. Since an electron traveling clockwise and counter clockwise has the same phase-winding (at zero magnetic field), the overlap of wave functions at the origin leads to positive interference and thus to an increased probability that the electron will be located at the origin. This so-called weak localization (WL) leads to a quantum correction of order h/e^2 to the resistance. The interactions between electrons and scatter centres also depend on the applied magnetic field. For a finite magnetic field time reversal symmetry is broken. Since all paths have a different magnetic flux enclosed, the phase of electrons will be different for each trajectory. This leads to destructive interference and thus does not lead to weak localization. Weak localization is featured by a higher resistance at zero magnetic field and upon applying a (small) magnetic field this resistance drops.

When the spin of electrons is taken into account, two electrons with opposite spin can travel the same trajectory. When no spin flip takes place, the electron waves travel independent from each other. However, in the case of spin-orbit coupling, the phase of the electron wave may change during an elastic scatter event. Since not every elastic collision leads to a spin flip, the spin orbit relaxation time (τ_{so}) is larger than the elastic scattering time, $\tau_{so} > \tau$. Due to the change of phase, the wave functions mix and are no longer independent. As long as the spin orbit relaxation time is smaller than the inelastic scattering time, $\tau_{so} < \tau_I$, the mixing of the wave functions leads to a negative correction to the resistance. This correction to the resistance is also known as weak antilocalization (WAL).

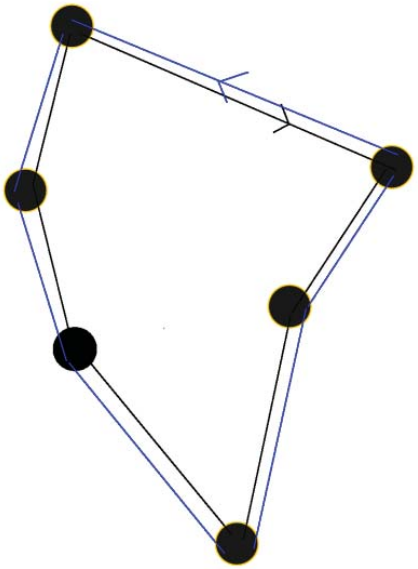

Figure 6.1: Sketch of electron waves traveling between scatter centres, opposite paths give rise to weak localization.

6.3 Spin orbit coupling

Since spin-orbit coupling may play a key role in the origin of superconductivity in the LAO/STO system, as discussed in Section 6.1, it is important to study it. It has been demonstrated that the spin orbit-coupling in LAO/STO can be tuned by applying a back-gate voltage[23, 24]. Back-gating has a few drawbacks, as discussed in Chapter 2, high voltages are needed, allowing for movement of oxygen or domain walls[2-4] and STO is known to have an electric-field (and temperature-) dependent dielectric constant[78]. To overcome these issues, we describe tunable spin-orbit coupling, using top-gating. We demonstrate that the spin orbit relaxation time is linked to the electric field rather than to the inverse of the elastic scattering time. Since the mobile carriers are in the d_{xz} *(*or d_{yz}*)* band and the spin-orbit coupling also originates from this band, this supports a coupling between superconductivity and spin-orbit coupling.

The experiments described in this work have been performed in a Physical Properties Measurements System (PPMS) at a temperature of T = 2 K. Measurements have been done in perpendicular magnetic field on a STO/LAO Hall-bar, where the LAO has a thickness of 12 unit cells. On top of the LAO gold was evaporated as a top-gate. . The gate voltage has been applied from the top-gate relative to the 2DEG. The magnetoresistance (MR) curves displayed in Fig. 6.2 show a clear dependence on top-gate voltage V_G.

The MR is defined as

$$MR = \left(\frac{R_S(B)}{R_S(0)} - 1\right) * 100\% \qquad (6.1)$$

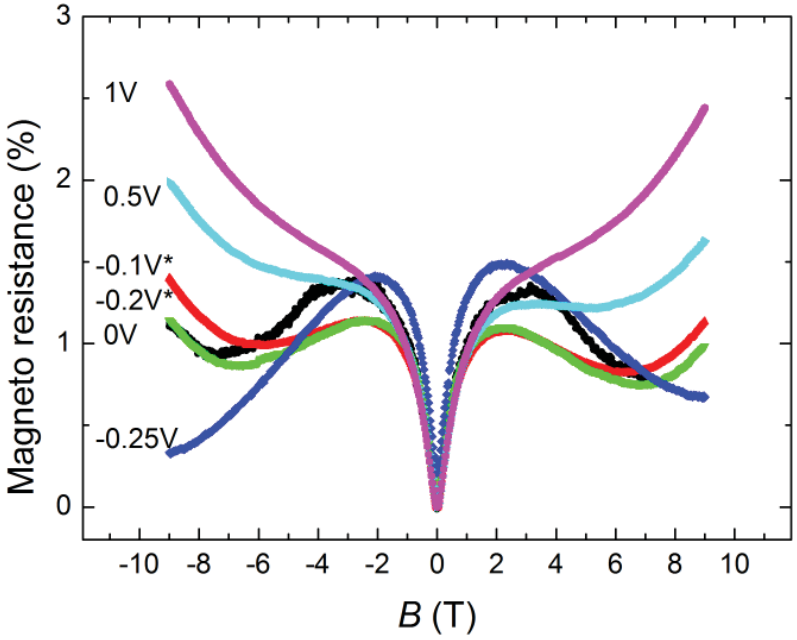

Figure 6.2: Magnetoresistance as a function of top-gate voltage. Measured at *T*=2K. The curves marked with a (*) at V_G= -0.1 and -0.2 V show measurements after cooldown in V_G= -0.2 V.

($R_s(0)$ being sheet resistance at zero field and R_s(B) the sheet resistance at an applied perpendicular magnetic field *B*). Depending on V_G the slope of the magnetoresistance curves is positive or negative at high magnetic field. Around *B*= 0 T a dip in the resistance is visible, indicating weak anti-localization. As discussed in section 6.2, weak anti-localization occurs in systems showing a strong spin-orbit coupling. Caviglia *et al.*[24] demonstrated that the LAO/STO interface has Rashba spin-orbit coupling and that the coupling can be tuned by means of back-gating. Following their analysis and the Maekawa-Fukuyama (MF) formula the spin orbit scattering could be calculated. The slightly modified Maekawa-Fukuyama (MF) formula is given by

$$\frac{\Delta\sigma(H)}{\sigma_0} = \Psi\left(\frac{H}{H_i+H_{so}}\right) + \frac{1}{2\sqrt{1-\gamma^2}}\Psi\left(\frac{H}{H_i+H_{so}(1+\sqrt{1-\gamma^2})}\right) - \frac{1}{2\sqrt{1-\gamma^2}}\Psi\left(\frac{H}{H_i+H_{so}(1-\sqrt{1-\gamma^2})}\right), \quad (6.2)$$

where $\Delta\sigma(H) = \frac{1}{R_S(H)} - \frac{1}{R_S(0)}$ is the correction to the conductivity due to weak localization, $\sigma_o = e^2/\pi h$ and $\Psi = \ln(x) + \psi(\frac{1}{2} + \frac{1}{x})$, where ψ is the digamma function. In this formula H_{so}, H_i and γ, are the fitting parameters, γ is defined as $\gamma = g\mu_B/4eDH_{so}$. Here *g* is the g-factor,

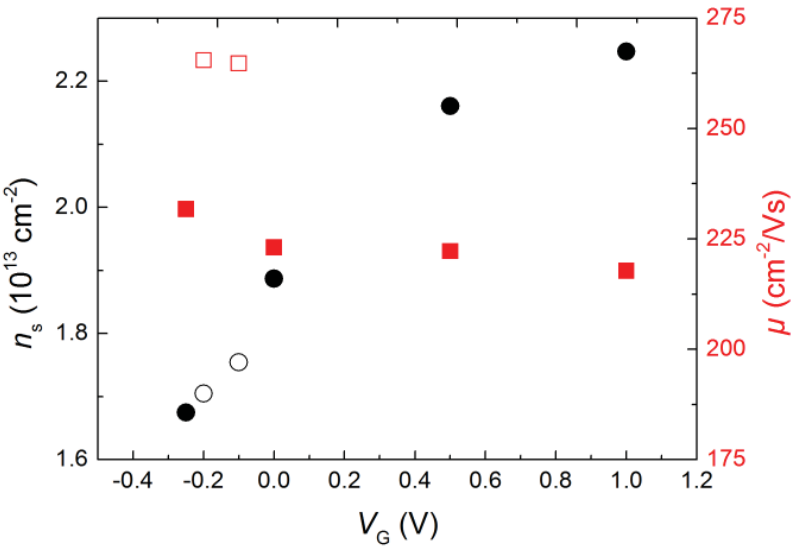

Figure 6.3: Carrier density (black circles) and mobility (red squares) as function of top-gate voltage. The filled symbols show measurements after cooling in V_G= 0 V. The open symbols at V_G= -0.1 and -0.2 V, show measurements after cooldown in V_G= -0.2 V. Measured at T=2K

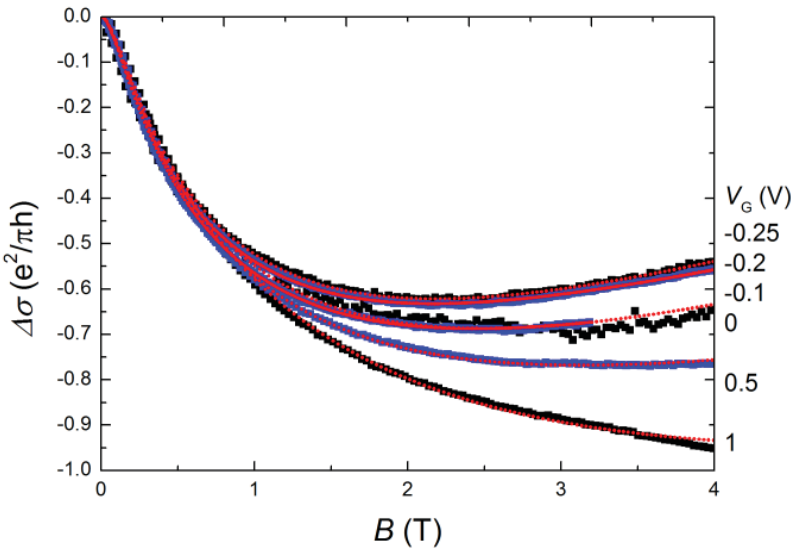

Figure 6.4: Best fits (red curves) to the correction to the conductivity according to the Maekawa-Fukuyama theory.

μ_B is the Bohr magneton, τ_{so} and τ_i are the spin-orbit relaxation time and the inelastic scattering time. $H_{so} = \frac{\hbar}{4eD\tau_{so}}$ and $H_i = \frac{\hbar}{4eD\tau_i}$ are the "spin-orbit field" and the "inelastic field" used for fitting the data and relate to the spin-orbit relaxation time and the inelastic scattering time, respectively. D is the diffusion constant. The diffusion constant has been calculated by $D=v_f\tau/2$, where v_f is the Fermi velocity and τ is the elastic scattering time. v_f can be calculated (for 2D systems) using $v_f = \frac{\hbar}{m}\sqrt{2\pi n_s}$ where n_s is the 2D carrier density. τ can be calculated using $\mu = \frac{|e|}{m}\tau$, where μ is the carrier mobility. The carrier density and

mobility to calculate those values have been measured in a Hall-bar configuration and are displayed in Fig. 6.3.

Figure 6.4 shows the best fits (lowest root mean square) according to the MF theory. Although the number of fitting parameters (3) is large, the effects of changing one of the three individual parameters can be discriminated on. Changing the "inelastic field" H_i, results in a deviation at low magnetic fields (B < 1 T), whereas the fit for high fields (B > 1 T) is mainly influenced by the "spin-orbit field" H_{so} and γ. The figure shows that choosing the correct fitting parameters leads to good fits for 0 T < B < 4 T. From the fitting parameters the spin orbit relaxation time τ_{so} and the inelastic scattering time τ_i can be deduced. These numbers have been shown in Fig. 6.5 as a function of V_G. The inelastic scattering time varies between 8 and 10 ps for all measured V_G and does not show a clear dependence on V_G. The spin-orbit scattering time increases for increasing negative gate voltages (to 1 ps) and decreases for increasing positive gate voltage (to 0.4 ps).

The Rasbha coupling constant α is related to the spin-orbit scattering time by

$$\tau_{so} = \frac{\hbar^4}{4\alpha^2 m^2 2D}. \qquad (6.3)$$

Using this relation, the Rashba coupling constant α (as a function of V_G) could be calculated as displayed in Fig 6.6. From this plot it seems that upon increasing the gate voltage, the spin orbit coupling increases linearly. To explain the linear trend in Fig. 6.5, the origin of the coupling constant will be derived below. The coupling constant α can be deduced from the Rashba Hamiltonian $\mathcal{H}_{SO}$:

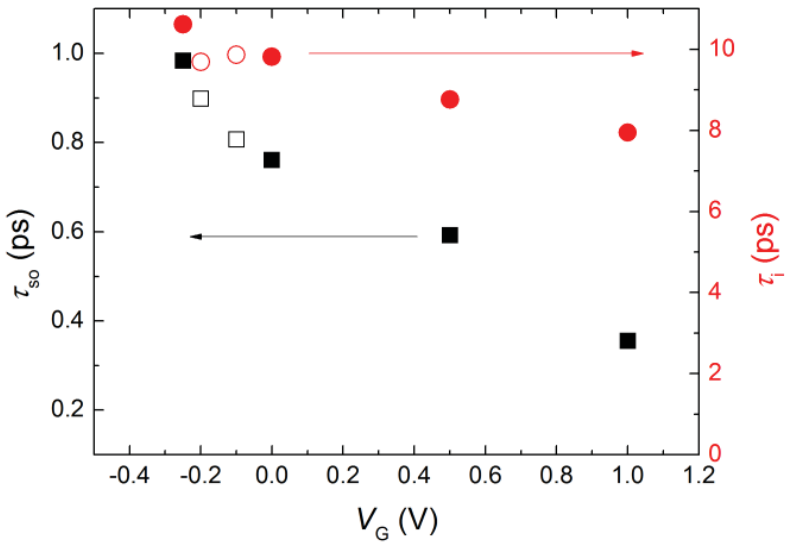

Figure 6.5: Left axis shows the spin-orbit relaxation time (black squares), right axis the inelastic scattering time (red circles) as function of V_G. The filled symbols show measurements after cooling in zero field. The open symbols at V_G= -0.1 and -0.2 V, show measurements after cooldown in V_G= -0.2 V.

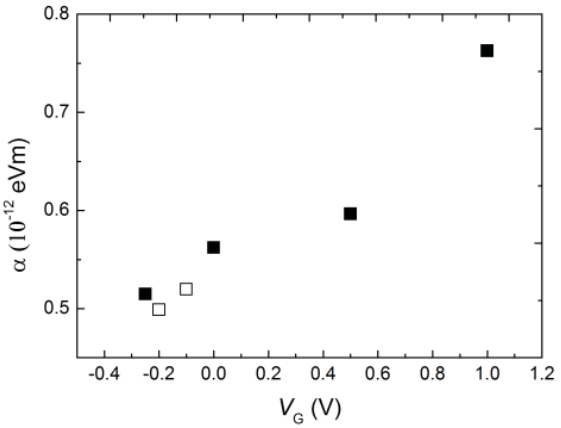

Figure 6.6: Rashba coupling constant α as function of V_G. The filled symbols show measurements after cooling in zero field. The open symbols at V_G= -0.1 and -0.2 V, show measurements after cooldown in V_G= -0.2 V.

$$\mathcal{H}_{SO} = \alpha(\vec{\sigma} \times \vec{k}) \cdot \vec{v} \tag{6.4}$$

Where $\vec{\sigma}$ is the Pauli vector matrix, $\vec{k}$ the wavenumber and $\vec{v}$ is the unit vector perpendicular to the surface. The spin orbit term in the Hamiltonian in the case of a two-dimensional system with an electric field in the $\vec{z}$-direction is given by:

$$\mathcal{H}_{SO} = g\mu_B \frac{1}{2c^2}\frac{\hbar E}{m}(\vec{\sigma} \times \vec{k}) \cdot \vec{v}\,, \tag{6.5}$$

where *c* is the speed of light and *E* is the effective electric field. Now coupling constant α is given by:

$$\alpha = g\mu_B \frac{1}{2c^2}\frac{\hbar E}{m}. \tag{6.6}$$

The effective field *E* is given by a constant electric field (E_0) (due to the symmetry breaking at the LAO/STO interface) and the contribution from the gate-voltage:

$$E = E_0 + \frac{V_G}{d}, \tag{6.7}$$

where *d* is the thickness of the LAO. Inserting 6.7 in 6.6 gives:

$$\alpha = g\mu_B \frac{1}{2c^2}\frac{\hbar}{m}(E_0 + \frac{V_G}{d}). \tag{6.8}$$

So the linear increase in spin-orbit coupling with increasing V_G as observed in Fig. 6.5 is in agreement with the expectations.

In back-gating experiments on spin-orbit coupling in LAO/STO a non-linear relation between α and V_G has been observed[24]. This may be related to the fact that the effective electric field is altered by the dielectric constant of STO, which changes with applied electric field, whereas the dielectric constant of LAO is constant under applied field.
It is remarkable that for top-gated measurements on the LAO/STO interface the V_G dependence of α, τ_{so}, τ_i and $\Delta\sigma_o$ is very similar to back-gated measurements both in value as in behavior.

6.4 Relaxation mechanisms

To investigate the mechanism of the spin-orbit relaxation, the relationship between the elastic scattering time τ and τ_{so} needs to be determined. In case of a Dyakonov-Perel[74] mechanism τ_{so}~1/ τ. This type of spin relaxation can originate from a discontinuity in the lattice, for example at an interface, as may very well be the case in LAO/STO[24]. In case of Elliot-Yafet[79, 80] (EY) spin relaxation, a linear relation is expected τ_{so}~ τ. EY-type of spin-orbit coupling originates from spin-orbit interaction from the conduction electrons with lattice ions.
A value for the effective mass is needed in order to calculate the elastic scattering time and the spin-orbit coupling constant, using the measured mobility. Following the analysis of Caviglia *et al.*[24] we assume *m,* the effective electron mass to be 3 m_e, m_e being the bare electron mass. A constant mass implies a single-band model, as is clear from Fig. 5.2, this is a valid assumption for this sample.
The mechanism, as deduced from the relation between the elastic and spin-orbit scattering times, is different. The dependence of the mobility on top- and back-gating is also different and these two may be coupled. For back-gating a negative gate voltage leads to lower carrier density and lower mobility[66]. For top-gating a negative gate voltage leads to lower carrier density, whereas the mobility remains constant, see Fig. 6.3. The elastic scattering time τ is deduced from the mobility and will be larger with increasing carrier density for back-gating, but remains constant with increasing carrier density when the gating has been done by top-gating. In other words, while there is a dependence of the elastic scattering time on the back-gate voltage, there will not be any dependence for top-gating. Since τ does not change, there is no dependence of τ_{so} on τ, so the relaxation mechanism cannot be determined for top-gating. For back-gating the mobility (and thus the elastic scattering time) does change with applied electric field: the mobility goes down when negative gate voltages are applied and down with positive gate voltages. Since the spin orbit relaxation time for back-gating is the same as discussed here for top-gating, Caviglia *et al.*[24] found a τ_{so}~1/ τ relation and concluded that the relaxation should be governed by the Dyakonov-Perel mechanism.

To investigate the influence of the elastic scattering time, the sample has been cooled down with an applied electric field of V_G= -0.2 V. This lead to a slightly higher mobility (longer scattering time) of about 265 cm^2/Vs at V_G= -0.2 V. (This higher mobility is probably a cooldown to cooldown difference.) Measurements were done at V_G= -0.2 and -0.1 V with this longer elastic scattering time. The carrier density and mobility of these measurements is displayed in Fig. 6.3 as open symbols.

As can be seen from Fig. 6.5 the observed τ_{so} and τ_i show a V_G dependence that is in line with previous measurements. Also the dependence of τ_{so} and τ_i on the carrier density, is in line with previous measurements, as is shown in Fig. 6.7 where the spin-orbit coupling time is plotted as function of the inverse of the carrier density, this relation is linear. Thus, the longer elastic scattering time τ does not influence the spin-orbit relaxation time in our measurements.

6.5 Effective mass

When we have a second look on the formulas we see that the mobility $\mu = \frac{|e|}{m}\tau$, and thus the elastic scattering time τ, are related with the effective mass m. At the same time the spin-orbit relaxation time also has a relation with m, since it is given by $\tau_{so} = \frac{\hbar^4}{4\alpha^2 m^2 2D}$. Now we assume the Rashba coupling constant α to be constant (α=1 x 10^{-12} meVm) and calculate the effective mass m as a function of V_G. The results are normalized to m_e, the bare electron mass, and displayed in Fig. 6.8. As expected, the effective mass follows a same trend as the Rashba coupling constant did in Fig. 6.6. The assumption that the effective mass depends on applied electric field is reasonable, since the electric field may lead to band bending at the interface. A different curvature of the electronic bands means a different density of states at the Fermi level and thus a different effective mass.

A better method would be extracting the effective mass from Shubnikov-de Haas oscillations. Unfortunately, the mobility of the sample investigated was too low to observe these.

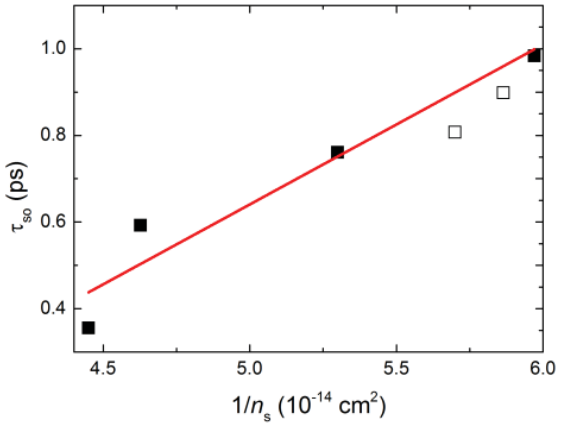

Figure 6.7: Spin orbit relaxation time as a function of carrier density, showing a linear relation. The open symbols at V_G= -0.1 and -0.2 V, show measurements after cooldown in V_G= -0.2 V.

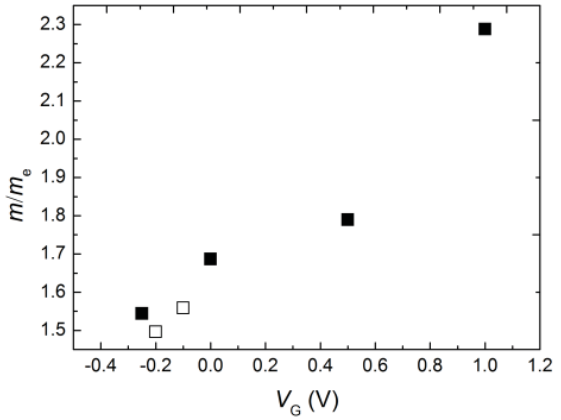

Figure 6.8: Gate voltage dependence of the effective mass

6.6 Temperature dependence

The temperature dependence of the magnetoresistance at a fixed gate-voltage (V_G= -275 mV) is displayed in Fig. 6.9. The weak anti localization peak becomes smaller and disappears with increasing temperature (at T = 10 K) and the slope of the magnetoresistance curve changes from negative to positive at high fields. On these data the same MF analysis can be made and values for the spin-orbit coupling time and the inelastic scattering times can be obtained. Since the spin-orbit relaxation time is temperature independent[81], the interesting information comes from the inelastic scattering times. At T = 10 K, the inelastic scattering time becomes smaller (0.5 ps) than the spin-orbit relaxation time (0.9 ps) and the weak anti-localization peak cannot be observed anymore.

Inelastic scattering can originate from several scattering mechanisms that have different temperature dependences. Main contributions come from electron-phonon scattering or electron-electron interactions. Figure 6.10 shows the inverse inelastic scattering time $1/\tau_i$

as function of the temperature. The observed linear dependence indicates that electron-electron interactions in a 2 dimensional system are the main source of inelastic scattering[82].

At first sight it may be counterintuitive that electron-electron interactions are indicated here as the main source of inelastic scattering and still the mobility does not change under the influence of an electric field. Whereas in Fig. 6.3 it has been shown that the carrier density (electrons) does change under influence of an applied electric field. Although electron-electron interactions are the main source of inelastic scattering, the mobility is not influenced, since the mobility is determined by the elastic scattering time.

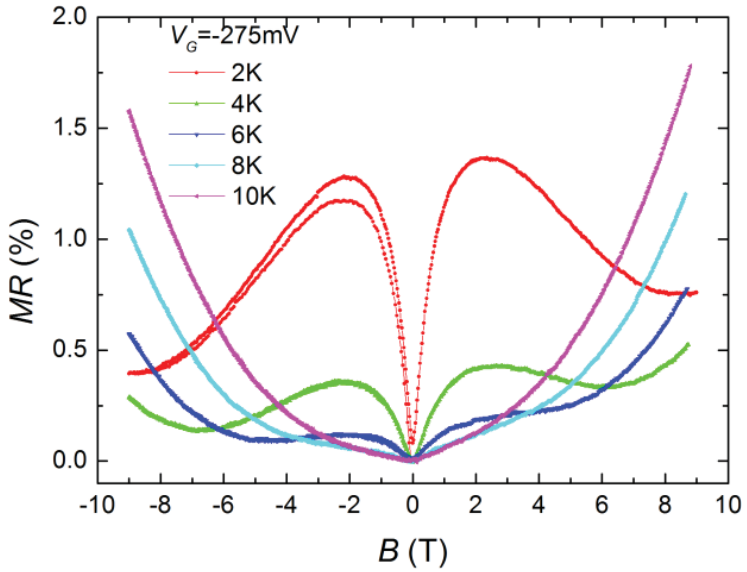

Figure 6.9: Temperature dependence of the Magneto resistance for a fixed gate voltage of V_G= -275 mV

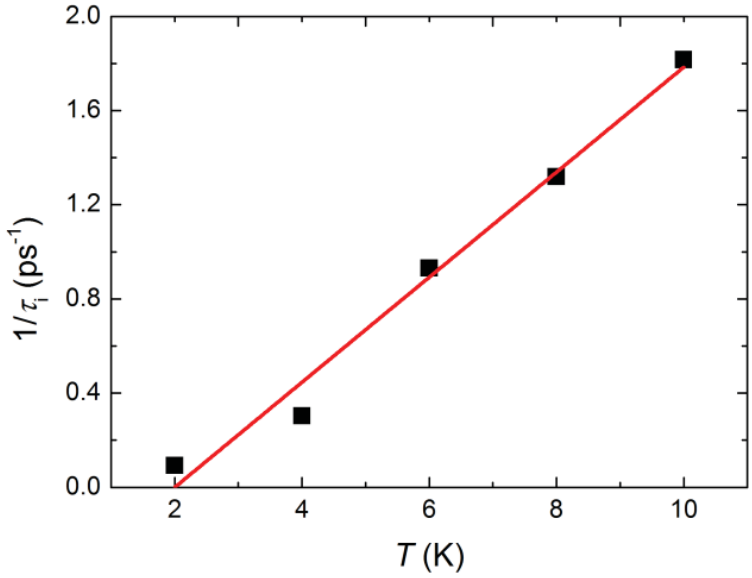

Figure 6.10: Inverse inelastic scattering time $1/\tau_i$ as function of the temperature. The solid line shows the linear dependence.

6.7 Discussion and conclusion

In summary we have measured the top-gate voltage dependence of the spin orbit relaxation time. This shows a decreasing τ_{so} when V_G and n_s are increasing, in agreement with previous studies[24]. The dependence of the spin-orbit coupling constant on the elastic scattering time could be fitted with neither the Dyakonov-Perel nor the Elliot-Yafet coupling mechanisms, since the elastic scattering time is constant as a function of gate voltage. Hosoda *et al.*[53] have reported a different mobility (and thus elastic scattering time) behavior on the top-gate voltage, namely a higher mobility with decreasing carrier density. If we would have measured the same, we most likely would have found the Elliot-Yafet coupling mechanism to be dominant in disagreement with the work of Caviglia *et al.*[24] since they reported the Dyakonov-Perel to be the dominant coupling mechanism in their study on back-gated spin orbit coupling.

Since back-gating has a strong influence on the conductivity at the interface and domain walls of the STO[2-4], it is likely that this effect causes the mobility dependence of the back-gate-voltage. In the top-gated system described here, no effect of the gate on the mobility has been observed, since the electric field is not across the STO, but instead across the LAO. Intuitively, one therefore would not expect any dependence of the mobility on the top-gate voltage, since the electric field does not influence scatter centers. (Only at very high carrier densities, where electron-electron interactions are the dominating scatter mechanism, or at very low carrier densities, where localization plays a role; a strong dependence of the mobility on carrier density is expected.)

Under the assumption of a constant effective mass, we demonstrate that the spin-orbit coupling constant α can be tuned, under the influence of an electric field. When we assume a constant coupling constant, a change in effective mass would be needed to fit the spin orbit relaxation time, according to equation 6.3. Since the coupling constant is known to depend on the electric field (see equation 6.6), the assumption of a constant coupling constant to obtain the effective mass is hard to defend. It is more likely that α is the parameter that can be tuned by applying a gate voltage.

In Fig. 6.6 we showed that α increases upon applying a positive electric field. In Chapter 5, it has been demonstrated (on the same device, see Fig. 5.6) that a positive electric field increases the critical current and critical temperature, when the sample is in the superconducting state. Since the critical current increases when the spin orbit coupling is stronger, it may very well be that the spin-orbit coupling in the d_{xy} electrons, acts as a mediator for superconductivity in the d_{xz} or d_{yz} electrons[24].

A future study on the spin-orbit coupling under influence from a combination of top-gating and back-gating could provide an answer to the question what the exact coupling mechanism is in this material system.

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Appendix A

List of abbreviations and symbols

α	Rashba coupling constant
ε	Dielectric constant
ε_0	Permittivity of vacuum
μ	Carrier mobility
μ_B	Bohr magneton
v_f	Fermi velocity
σ	Stefan's constant (σ = 5.67*10^{-8} Js^{-1}m^{-2}K^{-4})
$\Delta\sigma$	Correction to the conductance
τ	Elastic scattering time
τ_i	Inelastic scattering time
τ_{so}	Spin orbit relaxation time
ω_c	Cyclotron frequency
2DEG	Two-dimensional electron gas
AFM	Atomic force microscope
a-LAO	Amorphous $LaAlO_3$
B	Magnetic field
C	Capacitance
D	Diffusion constant
d_{LAO}	Thickness $LaAlO_3$ insulator
DP	Dyakonov-Perel
e	Elemental electric charge
EY	Elliot-Yafet
FET	Field effect transistor
g	g-factor
HAXPES	Hard x-ray photoemission spectroscopy
H_i	Inelastic field
H_{so}	Spin orbit field
I_G	Gate current
I_{SAT}	I_{SD} at V_{SAT}
I_{SD}	Source drain current
k_B	Boltzmann constant
L	length of the conducting channel between the voltage probes

LAO	$LaAlO_3$
LTO	$LaTiO_3$
MBE	Molecular beam epitaxy
m_e	Effective carrier mass
MR	magneto resistance
MF	Maekawa-Fukuyama
NDC	Negative differential conductance
n_s	Carrier density
P	Power
PFM	Piezo force microscopy
PLD	Pulsed laser deposition
PPMS	Physical Properties Measurements System
Q	Total charge
RHEED	Reflective high energy electron diffraction
R_{SD}	Source drain resistance
R_{xx}	longitudinal resistance
R_{xy}	Hall resistance
SMU	Source Measure Unit
STO	$SrTiO_3$
T	Temperature
T_C	Superconducting critical temperature
u.c.	Unit cell
V_G	Gate voltage
V_{SAT}	Maximum value of the *V(I)* curve
V_{SD}	Source drain voltage
W	Width of the channel/Hallbar

Appendix B

Process flow

B.1 Substrate treatment.

The substrates are cleaned by ultrasonic cleaning for 10 minutes in acetone and ethanol. Since acetone dries very quickly, the transfer from acetone to ethanol is done while having a big droplet of acetone on top of the substrate before transferring. After the ethanol cleaning, the substrate is blown dry with nitrogen and checked under an optical microscope. If present, particles are removed by sliding the polished side of the substrate on a lens tissue that has been wetted in ethanol. The sample is dried again by a nitrogen flow and inspected again optically, until no particles are left. The sample is then put in demineralized water for 30 minutes in an ultrasonic bath. In this time the SrO at the surface is hydrolyzed to SrO:OH. This dissolves in Hydrofluoric acid (HF). The sample is put in a buffered solution of 87.5% HF for 30 seconds in an ultrasonic bath. To remove the acid, the sample is put in 3 beakers of water for 30 seconds each. Finally the sample is put in ethanol and the samples are dry blown. To obtain straight step edges, the sample is put in a tube oven. With an oxygen flow of 150 L/h, the samples are heated to 950 ^{o}C and annealed there for a period of 90 minutes. For substrates with a small miscut angle (large terrace width), 90 minutes is not enough to get sharp edges. So for samples with a terrace width larger than 200 nm, the anneal time is increased to 120 minutes. After the anneal step the samples are investigated by atomic force microscopy, to see whether the steps are straight and no SrO is left at the step edges.

B.2. Structuring the 2DEG by a-LAO.

A positive resist 907/17 is spin coated to the sample. The sample is rotated for 35 seconds in total with a speed of 6000 rpm. In order to ensure uniform heating of the resist and a flat surface for additional photolithography steps, any residual photoresist is removed from the back of the sample by carefully cleaning it with a clean-room tissue that has been wetted with acetone. After this, the resist is hardened by placing it on a hot plate at 100 ^{o}C for 60 seconds. The sample is placed in the mask aligner and the mask is aligned to the alignment markers (if present). The sample is exposed for 6 seconds in hard contact mode. The resist is developed in developer OPD for 60 seconds. The development is stopped by rinsing the sample in 2 beaker glasses filled with clean demineralized water for 30 seconds each.

After applying a photomask to the sample, 10 nm[iii] amorphous $LaAlO_3$ (a-LAO) is deposited by PLD at room temperature at a pressure of $2x10^{-3}$ mbar at a frequency of 5Hz. The sample is glued on the heater by double sided tape. Tape has been chosen instead of silver paint, since the photoresist hardens and cannot be removed when the silver paint is heated to remove solvents from it. After lift off and careful cleaning in ultrasonic acetone and ethanol, the sample is glued to the heater with silver paint. After pre-ablation of the target at room temperature, the substrate is (also at room temperature) aligned to the RHEED beam. The system is heated to 850 ^{o}C. At that temperature the LAO deposition takes place. To control the thickness, this deposition is monitored by RHEED (see Section 3.4.4). After deposition, the system used to be cooled down to room temperature in deposition pressure, with a ramp rate of 10 ^{o}C/min.

The problem with this way of structuring is that a-LAO deposited on STO also gives rise to conductivity when deposited under certain conditions[13]. In order to resolve this issue, we included a 1 hour post anneal in high oxygen pressure (600 mbar) at 600 ^{o}C after the growth of crystalline LAO at 850 ^{o}C. This increases the resistance of the a-LAO from 1 MΩ (without post anneal) to over 50 GΩ (with post anneal) at room temperature.

The cooldown procedure used for the top-gated devices after deposition at 850 ^{o}C was cooldown in deposition pressure to 600 ^{o}C at a cooldown rate of 50 ^{o}C/min. At around 650 ^{o}C (in order to avoid the temperature to drop below 600 ^{o}C) the chamber was flooded with oxygen (about 400 mbar). The temperature was stabilized at 600 ^{o}C and after 1 hour annealing the sample was cooled down to room temperature at a rate of 50 ^{o}C/min, and it was removed from the system when the temperature was below 75 ^{o}C.

Contacts to the 2DEG are made by sputter depositing titanium/gold. High sputtering power is needed to ensure a good contact between the 2DEG and the gold contacts, (which would not be possible with e-beam evaporation, where the gold would not penetrate the LAO and the latter would form a barrier). After applying a photoresist layer, the samples are loaded in the sputter-system. When the background pressure is below 8 x 10^{-7} mbar, the argon process gas is added to the deposition chamber, resulting in a process pressure of 2 x 10^{-2} mbar. The titanium target is cleaned first for 2 minutes. Then the deposition of titanium at a power of 500 W is done for 15 seconds. After this, gold is deposited during 3 minutes at a power of 150 W. This leads to a layer thickness of about 100 nm.

After another photolithography step, the top-electrodes have been deposited via e-beam evaporation. In order to avoid shorts to the 2DEG, the gold has been evaporated at a rate of 0.2 Å/s for the first 20 nm and with a higher evaporation rate of 1 Å/s for the last 80 nm. No adhesion layer has been used.

[iii] a-LAO thicknesses of 100 nm and 26 nm, followed by a post anneal of 1h in 400 mbar O_2 resulted in a conducing path between adjacent structures.

Outlook

When I started working on LAO/STO at the beginning of 2010, the mechanism behind the conductivity between these two insulators was heavily debated. For the research described in this thesis it was not necessary to take part in this discussion. This thesis is more applied, in a sense that we accepted the presence of the 2DEG, although we did not understand every detail of it. And we started designing structures, devices with it.

The goal of the research was to design and make a structure in LAO/STO with a top-gate that can influence the properties of the 2DEG at the interface between LAO and STO.

In literature a method had presented to fabricate a device structure in LAO/STO. However copying this was not as easy as expected, since the growth procedure for the LAO was different from the method that is commonly used in our labs. For the Hall-bar fabrication the inclusion of a post-anneal in high oxygen pressure after the growth of crystalline LAO was necessary to have a well-defined structure.

The key improvement in the top-gate fabrication was the choice to use e-beam evaporation for the deposition of the gold top-gate electrode. This deposition method ensures a soft landing of the gold atoms on the LAO surface.

As a result the measured gate current density was record low. Furthermore it was shown that a gate voltage can influence the conductivity at room temperature and also at low temperatures.

A negative top-gate voltage decreases the carrier density, whereas a positive top-gate voltage enhances it. This is in agreement with back-gating experiments. It has been shown that the carrier density at zero gate voltage is comparable with samples without back-gate, so the gold electrode on top of the LAO does not influence the carrier density.

The superconductivity in the sample can be modulated by the application of an electric field via the top-gate. An increase in critical temperature and critical current density of the 2DEG can be observed when a positive gate voltage is applied. In back-gating studies hundreds of Volts need to be applied to see an effect on the superconducting critical temperature. Whereas in this work only voltages below 2 V were used to observe an increase in the critical current and critical temperature. It is the first time that it has been demonstrated in the LAO/STO material system that the superconductivity can be modified by applying an electric field from a top-gate.

Magnetotransport data was used to model the spin-orbit coupling in the LAO/STO system. It was demonstrated that a top-gate can influence the spin-orbit coupling in a similar way as a back-gate can, again with much smaller Voltages. The mobility that I determined as a function of gate voltage was almost constant at low temperature. This made it impossible

to link the elastic scattering time and the spin-orbit relaxation time. This relation would tell the mechanism behind the spin-orbit relaxation.

In the thesis I already made some specific suggestions for future research, such as the use of a different top-gate metal, investigation of the growth pressure dependence of the LAO on the tunnel current, and determining the tunnel mechanism. Open questions exist on the persistent insulating state at low temperatures when a negative gate voltage is applied, and on the oscillations observed in magneto transport. A combination of top and back-gating should resolve open question on the spin-orbit coupling.

The combination of top and back-gating is a direction that needs to be investigated for more reasons. The back-gate can globally lower or enhance the carrier density, whereas the top-gate can do this on a local scale. The combination of these effects can perhaps enhance the superconducting properties of the LAO/STO.

The fact that top-gating is possible allows for smaller top-gates, made by e-beam lithography. These local gates should be able to define nanowires or quantum dots in the LAO/STO system.

From an application point of view investigating the pressure dependence of the tunnel current may be interesting. Also the surface sensitivity could be investigated more, especially the adhesion of gasses on the LAO and the influence of this on the transport properties. LAO/STO might work as a gas sensor in that sense.

In my opinion the biggest challenge for the field of LAO/STO is to find a different substrate to deposit the devices on. Since, at this moment the quality of the STO substrates that are bought from suppliers varies strongly, and so does the mobility. A constant quality is needed and therefore the STO substrate needs to be replaced by STO that has been deposited on a different substrate.

Summary

Conductivity has been shown to appear in the form of a two-dimensional electron gas (2DEG) at the interface between the transparent, insulating materials $LaAlO_3$ and $SrTiO_3$. The LAO needs to be deposited on TiO_2 terminated STO, where a LAO thickness of at least 4 unit cells (u.c.) is required to observe conductivity. The origin of the conductivity is heavily debated, main candidates are oxygen vacancies at the STO surface or an electronic reconstruction, that resolves the potential buildup that is present in unreconstructed LAO due to the polar nature of the LAO.

The conductivity and related properties, such as carrier density and mobility can be tuned by adding additional top-layers on the LAO surface. Depending on the choice of materials, carrier density and/or mobility are enhanced or worsened.

Not only conductivity is present at the interface, the properties of the 2DEG are more diverse. If the mobility is high enough quantum oscillations and universal conductance fluctuations can be observed in magnetic field. Furthermore magnetism, and superconductivity have been reported. It has been suggested that the observed spin-orbit coupling plays a crucial role in explaining the co-existence of both phenomena.

The properties, such as spin-orbit coupling and superconductivity can be tuned by means of a back-gate voltage. However, back-gating changes the domain structure of the STO substrate, thereby changing the conductivity at the interface not only due to the electric field but also due to this chance in structure.

This thesis focusses on making a top-gated device in LAO/STO that would enable us to tune the properties on a more local scale, with lower gate voltages and without moving domains.

A field effect transistor consists of 3 main elements: the source drain channel, the gate insulator and the gate itself. In order to make a FET in an oxide 2DEG, control is needed on each of the individual components. The structuring of the 2DEG had to be done by using a hard mask of amorphous LAO. This a-LAO is not conducting when a post anneal in high-oxygen pressure is applied after deposition of the crystalline LAO. As a gate-dielectric we choose to use LAO and not add additional dielectrics, as they might alter the properties of the 2DEG. The addition of parylene as a buffer layer made the required voltages to observe a chance in resistance higher, due to the larger distance, leading to a significant gate current. For the final top-gated device, we used gold for the top-gates that was deposited directly on LAO and was evaporated via e-beam evaporation, since sputtering led to shorts.

For an ideal gate, no current flows between gate electrode and 2DEG. In chapter 4 it was demonstrated that, for sample with a LAO insulator thickness that exceeds 10 u.c., the

gate current is less than 2 nA for all applied negative gate voltages. This can be explained by the fact that a negative gate voltage depletes the 2DEG. When a thin dielectric is used, a significant current can flow from the top-electrode to the 2DEG. This current shows clear hysteresis and a negative differential resistance, which can be explained by a competition between tunnel current and depletion of the 2DEG. Lowering the temperature raises the tunnel current. This is also the case when the sample is placed in vacuum. The exact reason why this happens, is unclear, but it may be related to adsorbents (water) or oxygen vacancies in the LAO.

When LAO is grown with a thickness of 11 u.c., the LAO is a good dielectric and the conductivity can be switched on and off within a second with a low gate voltage (V_G = -0.8 V). Furthermore the carrier density and carrier mobility, as extracted from $I(V)$ measurements can be tuned by the gate voltage. The observed carrier density and mobility are in agreement with measurements at room temperature in a magnetic field.

At low temperature gating is possible in a small voltage regime: -0.5 V < V_G < 1.5 V, since the gate current increases outside this regime. This increase outside the working regime in gate current leads to power dissipation, leading to a local increase in temperature. The capacitance of the (12 u.c.) LAO layer could be calculated by determining the carrier density from the Hall resistance. From the capacitance, the dielectric constant of LAO could be determined to be 7, lower than the bulk value, but in agreement with thin film data.

Below 240 mK the 2DEG becomes superconducting. This superconductivity can be tuned by top-gating. A positive gate voltage raises the critical temperature and critical current, whereas a negative gate voltage lowers it. A large enough negative gate voltage brings the 2DEG in an insulating state. Once this insulating state is reached, the system cannot recover from it, unless it is heated to a temperature exceeding 160 K.

Small negative gate voltages can also lead to quantum oscillations in the magneto resistance, that are periodic in 1/B.

It has been reported that the spin orbit coupling in LAO/STO can be tuned by applying an electric field by means of back-gating. Chapter 6 describes the analysis of magnetotransport data as a function of top-gate voltage. The dip in resistance (weak anti-localization) around zero magnetic field, could be fitted with the modified Maekawa-Fukuyama formula. From the fitting the spin orbit relaxation time could be deduced. With increasing (positive) field the spin orbit relaxation time decreases, indicating a stronger spin orbit coupling. Since the mobility (and hence the elastic scattering time) of the electrons does not change with applied field, no discrimination could be made between the Elliot-Yafet and the Dyakonov-Perel relaxation mechanisms. From the inelastic scattering time dependence on the temperature, electron-electron interactions could be indicated as the main source for inelastic scattering at low temperatures.

In conclusion, this thesis describes the development of working top-gated STO/LAO 2DEGs. Those structures can be operated from room temperature down to milliKelvin temperatures. By applying a top-gate voltage, the conductivity in the source drain channel can be tuned. At low temperatures the superconductivity (critical temperature and critical current) can be enhanced by applying a gate voltage. Also an increase in spin orbit coupling strength has been deduced from measurements on the magnetoresistance. The ability to top-gate those 2DEGs opens the road towards deeper understanding of the mechanisms that play a role in the rich variety of the conductivity at the interface of these complex oxides. Furthermore, downscaling the top-gates can allow for local gating of the top-gate, a step needed towards realizing Nano scale quantum dots in complex oxides.

Samenvatting

Het is aangetoond dat er geleiding optreedt in de vorm van een tweedimensionaal elektronen gas (2DEG) aan het grensvlak tussen de transparante, isolerende materialen $LaAlO_3$ en $SrTiO_3$. Het LAO moet daarvoor gedeponeerd worden op STO met een TiO_2 getermineerd oppervlak, waarbij het LAO een dikte van ten minste 4 eenheidscellen moet hebben om geleiding te veroorzaken. Over de oorsprong van de geleiding wordt hevig gediscussieerd, belangrijkste kandidaten zijn zuurstofvacatures aan het STO oppervlak of een elektronische reconstructie, die de potentiaal opbouw in LAO oplost.
De geleiding en gerelateerde eigenschappen, zoals ladingdragerdichtheid en mobiliteit kunnen gemoduleerd worden door het toevoegen van extra toplagen op het LAO oppervlak. Afhankelijk van de materiaalkeuze kunnen de ladingdragerdichtheid en/of mobiliteit verbeterd of verslechterd worden.
Niet alleen geleiding is aanwezig aan het grensvlak, de eigenschappen van het tweedimensionaal elektronengas zijn divers. Als de mobiliteit hoog genoeg is, kunnen kwantum oscillaties en universele geleidings fluctuaties waargenomen worden in een magnetisch veld. Daarnaast zijn magnetisme en supergeleiding gerapporteerd. Het is gesuggereerd dat de geobserveerde spin-baan koppeling een cruciale rol speelt in het uitleggen van het tegelijkertijd bestaan van beide fenomenen.
De eigenschappen, zoals spin-baan koppeling en supergeleiding kunnen gemoduleerd worden door middel van het aanleggen van een gate-spanning aan de onderkant van het sample. Maar een spanning over het STO verandert de domeinstructuur van het substraat, waardoor de geleiding aan het grensvlak niet alleen door het elektrisch veld wordt veranderd, maar ook door deze verandering in de structuur.
Dit proefschrift focust op het maken van een LAO/STO structuur met top-gates, die het mogelijk maakt om de eigenschappen op een meer lokale schaal te beïnvloeden, met lagere spanningen en zonder last te hebben van bewegende domeinen.
Een veldeffecttransistor bestaat uit 3 belangrijke onderdelen: het geleidingskanaal, de gate isolator en de gate zelf. Om een veldeffecttransistor in een oxidisch 2DEG te maken, is controle nodig over elk van deze componenten. Het structureren van het 2DEG werd gedaan door het gebruik van een hard masker van amorf LAO (a-LAO). Dit a-LAO is isolerend wanneer er een verhitting in hoge zuurstofdruk plaatsvindt na de depositie van kristallijn LAO. Voor de gate isolator hebben we gekozen om geen extra diëlektricum te gebruiken, aangezien deze de eigenschappen van het 2DEG zouden kunnen beïnvloeden. Het toevoegen van paryleen als buffer laag leidde er toe dat hogere spanningen nodig waren om een verandering in weerstand van het 2DEG te induceren, door de grotere gate-

spanningen die nodig waren ten gevolge van de grotere afstand tussen gate en 2DEG. Voor de uiteindelijke structuur met top-gates hebben we goud gebruikt voor de top-gates. Dit goud is rechtstreeks op het LAO gedeponeerd met elektronenstraalverdamping, omdat sputteren van goud tot kortsluiting tussen het 2DEG en de gate leidde.

In het geval van een ideale gate is er geen stroom tussen de gate electrode en het 2DEG. In hoofdstuk 4 is laten zien dat voor een sample met een LAO laag van 10 eenheidscellen de gate stroom lager is dan 2 nA voor alle geteste negatieve gatespanningen. Dit kan verklaard worden door het feit dat een negatieve gatespanning het 2DEG depleert. Wanneer een dunne gate isolator gebruikt wordt, stroomt er een significante stroom tussen de top-electrode en het 2DEG. Deze stroom laat duidelijke hysterese zien en een negatieve differentiële weerstand, die verklaard kunnen worden door een competitie tussen tunnelstroom en depletie van het elektronen gas. Het verlagen van de temperatuur verhoogt de tunnel stroom. Dit is ook het geval wanneer het sample in vacuüm geplaatst wordt. De exacte oorzaak is niet duidelijk, maar het zou gerelateerd kunnen zijn aan absorbaten (water) of zuurstofvacatures in het LAO.

Wanneer de dikte van het LAO 11 eenheidscellen is, is het LAO een goed diëlektricum en de geleiding kan aan- en uitgeschakeld worden binnen een seconde met een lage gatespanning (V_G = -0.8 V). Bovendien kunnen de mobiliteit en ladingsdragerdichtheid, die geëxtraheerd kunnen worden uit $I(V)$-metingen, gemoduleerd worden met een gatespanning. De waardes die hieruit volgen zijn in overeenstemming met kamertemperatuur metingen gedaan in een magnetisch veld.

Op lage temperaturen is het aanleggen van een gatespanning mogelijk in een klein spanningsbereik: -0.5 V < V_G < 1.5 V, omdat buiten dit bereik de lekstroom snel toeneemt. Deze toename zorgt voor energie dissipatie en een lokale toename in temperatuur. De capaciteit van de (12 eenheidscellen dikke) LAO laag kon bepaald worden uit de ladingdragerdichtheid, die volgde uit het meten van de Hall-weerstand. Via de capaciteit kon de diëlectrische constante van het LAO bepaald worden: 7. Deze waarde is lager dan de bulk waarde, maar in overeenstemming met data gemeten in dunne lagen.

Het 2DEG wordt supergeleidend onder de 240 mK. Deze supergeleiding kan gemoduleerd worden met een top-gate. Een positieve spanning verhoogt de kritische stroom en kritische temperatuur, terwijl een negatieve spanning ze verlaagt. Een groot genoeg negatief veld brengt het 2DEG in een isolerende toestand. Zodra deze toestand bereikt is, kan het systeem hier niet uitkomen, tenzij het wordt verhit tot een temperatuur boven de 160 K.

Kleine negatieve gatespanningen leiden ook tot kwantum oscillaties in de magnetoweerstand, welke periodiek zijn in 1/B.

Het is gerapporteerd dat de spin-baan-koppeling in LAO/STO gemoduleerd kan worden door het aanleggen van een elektrisch veld via een back-gate. Hoofdstuk 6 beschrijft de analyse van magnetotransportdata als een functie van top-gatespanning. De dip in de

weerstand (zwakke anti-lokalisatie) rond nul magneetveld kon beschreven worden met een gemodificeerde Maekawa-Fukuyama formule. Uit de fits kon de spin-baan relaxatie tijd afgeleid worden. Met toenemende (positieve) veldsterkte neemt de spin-baan relaxatie tijd af, dit duidt op sterkere spin-baan koppeling. Aangezien de mobiliteit (en dus de elastische verstrooiingstijd) van de elektronen niet verandert met aangelegd veld, kan er geen onderscheid gemaakt worden tussen de Elliot-Yafet en Dyakonov-Perel relaxatie mechanismes. Uit de temperatuurafhankelijkheid van de inelastische verstrooiingstijd kan worden afgeleid dat elektron-elektron interacties de belangrijkste bron van inelastische verstrooiing op lage temperaturen zijn.

Concluderend beschrijft dit proefschrift de ontwikkeling van werkende STO/LAO 2DEGs met een top-gate. Deze structuren kunnen operationeel zijn van kamertemperatuur tot milliKelvin temperaturen. Door het aanleggen van een top-gatespanning kan de geleiding in het geleidingskanaal gemoduleerd worden. Op lage temperaturen kan de supergeleiding (kritische- stroom en temperatuur) verbeterd worden door het aanleggen van een elektrisch veld. Ook een toename in de sterkte van de spin-baan koppeling kan afgeleid worden uit metingen aan de magnetoweerstand. De mogelijkheid om een top-gatespanning aan te leggen op dit oxidische elektronen gas opent de weg naar een dieper begrip van de mechanismen die een rol spelen in de rijke variëteit van de geleidingseigenschappen aan het grensvlak. Bovendien zou het verder verkleinen van de top-gates het mogelijk maken om op een meer lokale schaal een gatespanning aan te leggen, een noodzakelijke stap richting nanoschaal kwantum eilanden in complexe oxides.

Dankwoord

Het dankwoord van proefschriften is aan inflatie onderhevig: meer en meer mensen “moeten” worden genoemd. Dit kan tot gevolg hebben dat de mensen die het belangrijkst zijn geweest voor het succesvol afronden van het proefschrift niet de aandacht krijgen die ze verdienen. Vandaar dat ik afwijk van deze traditie. Natuurlijk wil ik hierbij wel mijn begeleiders, technici, secretaresses en collega’s bedanken voor hun hulp.

I want to thank three of my colleagues specially, who really helped me during my Ph.D. project, without profit for themselves. Thank you, Tian Gang and Elia Strambini for helping me with experiments on the Heliox and Triton. Xiao Renshaw Wang, you were a really smart and helpful colleague. Thanks for the many conversations on LAO/STO, science in general, the cover design and “your” possible interviews on national radio.

Vriendschap is een van de belangrijkste dingen die er is en vriendschap heeft vele vormen. Met Paul en Frank heb ik tijdens mijn promotie minstens tien landen bezocht. Met Jarich heb ik vele nuttige gesprekken gevoerd. Maar bovenal heb ik altijd steun gekregen van jullie, bedankt daarvoor.

Onvoorwaardelijke steun en support heb ik gekregen van mijn ouders, broer en zus. Bedankt. Jullie opbeurende woorden zijn bij dit lastige project nodig gewest.

Uiteraard wil ik Margriet bedanken. Hoewel je het kortst van iedereen betrokken bent geweest bij het project, heb je er wel het meest last van gehad. Maar je hebt het geaccepteerd, begrip getoond en me enorm gesteund. Daar ben ik je heel erg dankbaar voor.

Mijn paranimfen Paul en Marco verdienen niet alleen een bedankje voor hun rol in de ceremonie. Jullie juiste woorden hebben ervoor gezorgd dat dit proefschrift gedrukt is en verdedigd mag worden. Bedankt daarvoor.

List of publications

Hard x-ray photoemission and density functional theory study of the internal electric field in SrTiO3/LaAlO3 oxide heterostructures

Slooten, E. , Zhong, Z., Molegraaf, H.J.A., **Eerkes, P.D.**, De Jong, S., Massee, F., Van Heumen, E., Kruize, M.K., Wenderich, S., Kleibeuker, J.E., Gorgoi, M., Hilgenkamp, H., Brinkman, A., Huijben, M., Rijnders, G., Blank, D.H.A., Koster, G., Kelly, P.J., Golden, M.S.
Physical Review B, Volume 87, Issue 8, 085128 (2013)

Modulation of conductance and superconductivity by top-gating in LaAlO 3/SrTiO3 2-dimensional electron systems

Eerkes, P.D., Van Der Wiel, W.G., Hilgenkamp, H.
Applied Physics Letters, Volume 103, Issue 20, 201603 (2013)

Effect of high oxygen pressure annealing on superconducting Nd 1.85Ce0.15CuO4 thin films by pulsed laser deposition from Cu-enriched targets

Hoek, M. , Coneri, F., Leusink, D.P., **Eerkes, P.D.**, Wang, X.R., Hilgenkamp, H.
Superconductor Science and Technology Volume 27, Issue 4, 044017 (2014)

Propositions

accompanying the thesis

Top-gating of the two-dimensional electron gas at complex oxide interfaces

Peter Eerkes

1. Gold top-gate electrodes deposited on $LaAlO_3/SrTiO_3$ with e-beam evaporation have low leakage currents. *(This thesis)*

2. The conductivity at the interface between $LaAlO_3$ and $SrTiO_3$ can be switched off by applying an electric field by means of a voltage on the top-gate electrode. *(Chapter 4 of this thesis)*

3. The superconducting critical temperature of the electron gas at the interface between $LaAlO_3$ and $SrTiO_3$ can be manipulated by applying an electric field by means of a voltage on the top-gate. *(Chapter 5 of this thesis)*

4. “Elk voordeel heb zijn nadeel” can be seen as an expression of the uncertainty relation of Heisenberg.

5. It would be beneficial for the quality of science when PhD-students play a role in the process of honoring research grants.

6. The “unique selling point” of a sport is at the same time the weakest point of that sport.

Stellingen

behorende bij het proefschrift

Top-gating of the two-dimensional electron gas at complex oxide interfaces

Peter Eerkes

1. Gouden top-gate-elektrodes gedeponeerd op $LaAlO_3/SrTiO_3$ met elektronenbundel opdamping hebben lage lekstromen. *(Dit proefschrift)*

2. De geleiding op het grensvlak tussen $LaAlO_3$en $SrTiO_3$ kan worden uitgeschakeld door het aanleggen van een elektrisch veld door middel van een spanning op de top-gate-elektrode. *(Hoofdstuk 4 van dit proefschrift)*

3. De supergeleidende kritische temperatuur van het elektronengas op het grensvlak tussen $LaAlO_3$ en $SrTiO_3$ kan gemanipuleerd worden door het aanleggen van een elektrisch veld door middel van een spanning op de top-gate. *(Hoofdstuk 5 van dit proefschrift)*

4. “Elk voordeel heb zijn nadeel” kan gezien worden als een uiting van de onzekerheidsrelatie van Heisenberg.

5. Het komt de kwaliteit van de wetenschap ten goede als promovendi een rol spelen in het proces van de honorering van een onderzoeksvoorstel.

6. Datgene wat een sport uniek maakt, is tegelijkertijd de grootste zwakte van die sport.